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Esmaeil Najafi Aghdam, Philippe Benabes. Reducing multibit DAC circuits errors by a simplified dynamic element matching algorithm used in delta-sigma converters. 15th ICEE - Iranian Conference on Electrical Engineering, May 2007, Iran. pp. 70-75. hal-00222968

HAL Id: hal-00222968

https://centralesupelec.hal.science/hal-00222968

Submitted on 29 Jan 2008

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Reducing multibit DAC circuits errors by a simplified dynamic element matching algorithm used in delta-sigma converters

Esmaeil Najafi Aghdam (1) , and Philippe Benabes (2)
(1) Dept. of Electrical Eng. Sahand Univ. of Tech. 51335-1996, Tabriz, Iran, najafiaghdam@sut.ac.ir
(2) Dept. of SSE, SUPELEC, Plateau de Moulon, Gif sur Yvette, 91192, Franc, Philippe.Benabes@supelec.fr

***Abstract*— Resolution of a multibit delta-sigma modulator (DSM) is limited by its internal digital-to-analog converter (DAC) nonlinearity that is usually caused by circuit mismatch errors while realizing. Recently, some dynamic element matching (DEM) methods were proposed for reducing mismatch errors. Two main difficulties of different dynamic element matching (DEM) techniques relate to instability and complexity of their algorithms. This paper provides a general method to simplify and to improve stability of high order dynamic element matching algorithms. It is shown that the proposed modifications can reduce necessary hardware for any order of sorting DEM algorithms and improve stability of the high order tree-structured DEM, without scarifying a considerable part of their ideal mismatch-shaping function. Simulations are presented for different 6^{th} and 4^{th}-order bandpass mismatch-shaping circuit, moved inside the feedback loop of a 6^{th}-order bandpass delta-sigma modulator. However, it can also be used in lowpass DSM.**

I. Introduction

With increasing demand of $\Delta\Sigma$ modulators (DSMs) with broader bandwidth and wider dynamic range (DR), multibit architectures become attractive for this trend as [1], [2]:

- the SNR directly increases by $6dB$ for each extra quantization bit, resulting in lower OSR application possible,
- multibit DSM's loop possesses better stability resulting in additional loop gain for higher order structure, which in turn results indirectly in improved SNR,
- it is one of the best ways to reduce clock jitter noise resulting in high frequency application possible,
- it possesses lower idle tone and lower out of band noise,
- in multibit DSM, the first opamp needs lower input range and slew-rate resulting in lower power consumption.

On the other hand, a multibit DSM needs a multibit-DAC on the feedback path which is usually a thermometric current steering DAC limited to 5-bits. Any feedback-DAC can suffer from inevitable mismatching occurred during fabrication process. This is a large disadvantage of the multibit DAC which seriously degrades its SNR, as it acts in the feedback path. Multibit architecture has no other sever inconvenience and its circuits' complexity can be accepted if one needs such many advantages mentioned above.
In order to integrate a multibit DSM, several error correction methods have been developed as trimming, calibration, digital correction, and dynamic element matching (DEM). The last one is widely used in high performance integrated modulators having a resolution over 10 bits. This technique can be realized in different ways. Randomization scheme whitens DAC's mismatch errors over whole frequency range, so that input depended tones are diminished but its noise floor increases in the band of interest. Thus, better solution can be using a mismatch noise shaping technique. The well-known data weighted averaging method (DWA) can effectively be used to shape mismatch errors reside in signal band. However, with the same frequency as in the quantizer, it can mainly be applied as a first order lowpass mismatch-shaping. For higher order mismatch-shaping, only two original methods have been introduced; feedback-vector or sorting algorithm ($SDEM$) [3] and tree-structured scheme ($TDEM$) [4]. The SDEM suffers from lower hardware efficiency and clock rate limits, especially for higher number of quantization level. The TDEM suffers more from algorithm instability for high order mismatch-shaping.
The authors have lately developed two new schemes, which are based on two mentioned original methods. The first one, called $MDEM$, is a mixed structured of SDEM and TDEM [5]. The MDEM benefits of better stability nature of SDEM and hardware efficiency of TDEM. The second one, called $STDEM$, is a shortened tree-structured introduced in [6]. It is more stable than the pure TDEM with the same hardware efficiency. This paper tends to further generalize these schemas and introduces some examples of its related circuits, which are designed for a 3-bit feedback-DAC, in two next sections.

II. Simplified dynamic element matching algorithm

The proposed algorithm is based on conventional TDEM [4] using an adapted segmenting strategy [7]. Figure 1 shows the general block diagram of a B-bit segmented tree-structured DAC, where each of the s segments employs an M-level sub dynamic element matching (Sub-DEM) algorithm. In order to explain the proposed algorithm, first we need to rewrite some basic equations for a TDEM algorithm [4], as in the left side of the schematic shown in figure 1.
A conventional pure TDEM maps each digital input, supposed

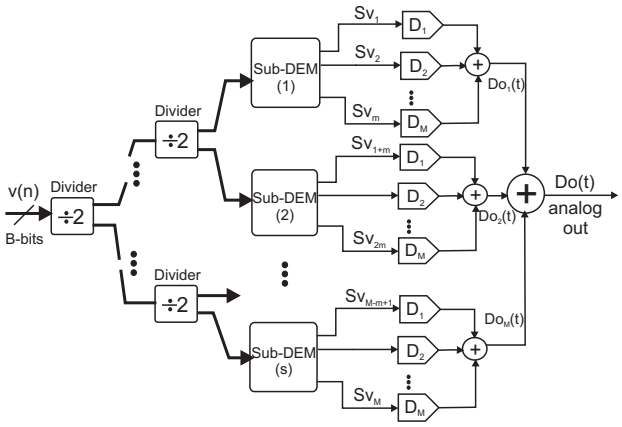


Fig. 1. Proposed Dynamic element algorithm matching with a segmented strategy.

B bit binary code $Y(n)$ which comes from an internal flash-ADC, to an M-element vector $SV(n)$. The TDEM consists of some $layers$ shown as different columns. Each layer also consists of some boxes laid out in rows. All boxes within the tree structure are called switching blocks and are labeled $S_{k,r}$, where k denotes the layer number and r denotes the position of the switching block in the layer. As a general case, these blocks can also be called *Divider Block (DB)*. Each divider block $S_{k,r}$ has a $(k+1)$-bit input y_{kr} and two k-bit output $y_{k-1,2r-1}$ and $y_{k-1,2r}$. For each y_{kr} input, these restrictions are explained by the following equations:

$$\begin{cases} y_{k-1,2r-1} &= (y_{kr}+s_{kr})/2 \\ y_{k-1,2r} &= (y_{kr}-s_{kr})/2 \end{cases} \quad (1)$$

In order to fulfill number conservation rule and to be compatible with the rest of algorithm, $s_{kr}(n)$ must satisfy certain conditions for number conservation rule, as:

$$\begin{aligned} s_{kr}(n) &= \begin{cases} \text{even} & \text{if } y_{kr} \text{ is even} \\ \text{odd} & \text{if } y_{kr} \text{ is odd} \end{cases} \\ |s_{kr}(n)| &\le \min\{y_{kr}(n), 2^k - y_{kr}(n)\} \end{aligned} \quad (2)$$

In general, $s_{kr}(n)$ can be a fixed or variable value in each of odd or even case. In the following subsection, four different possibility for the DB blocks will be outlined.
On the other hand as will be shown later in this paper, the sub-dynamic element matching blocks shown in figure 1 can also be realized by different ways. We will also propose three practical types here in the blow.

III. Different kinds of divider blocks

In the simplest case, $s_{kr}(n)$ is set "0" for even and "1" for odd cases. In other word, the simplest form of a switching block is a divider wherein the rest of dividing operation has to be generally added on one of the output values. This type of DB does nothing as a mismatch-shaping process but simplifies the rest of algorithm which can use a restricted form of DEM, separately in Sub-DEM blocks.
In order to suppress unwanted tones rising by mismatched elements of a multibit DAC, the dividers may be designed to add its rest to one of its outputs in a random manner. Such a divider which may produce an equally distributed spectrum across the whole of the band, can also be called *randomly-divider block (RDB)*. This kind of DB is suitable in some cases depending on the order of DEM order. For example, a RDB can improve the performance of a partitioned random DEM algorithm [8]. However, in a first or higher order DEM algorithm, neither a fixed value nor random value for $s_{kr}(n)$ can effectively improve mismatch-shaping performance [6].
In an ideal case, $s_{kr}(n)$ must form a shaped sequence with minimum energy in the band of interest [9]. Its suitable structure, which is usually used in a TDEM algorithm and known as the switching block (SB), is shown in figure 2 [4].

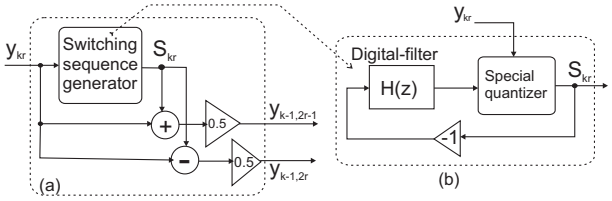


Fig. 2. a)Conventional SB's structure b)switching sequence generator

The special quantizer transfer function was first defined as:

$$s_{kr}(n) = \begin{cases} 1 & \text{if } y_{kr} \text{ is odd and } v_{kr} > 0 \\ -1 & \text{if } y_{kr} \text{ is odd and } v_{kr} < 0 \\ 0 & \text{in all other cases} \end{cases} \quad (3)$$

This definition imposes a very strict rule to produce $s_{kr}(n)$ sequences so that it takes only zero for any even SB's inputs. This in turn, can cause instability in the mismatch shaping loop and overflow can occur in the second and following stages of the filter if the input of the DB remains even for a few periods. To meet better stability, it was then modified [6], [10]:

$$S_{kr}(n) = \begin{cases} +1 & y_{kr} \text{ is odd and } v_{kr} > 0 \\ -1 & y_{kr} \text{ is odd and } v_{kr} < 0 \\ +2 & y_{kr} \text{ is even and } v_{kr} > 0 \\ -2 & y_{kr} \text{ is even and } v_{kr} < 0 \\ 0 & \text{in all other cases} \end{cases} \quad (4)$$

The above-mentioned modification results in better stability, but it is not applicable for the two last layer when m is set to "0". This is because the two first layers' inputs can only lie between [0,4] thus, equation 4 recalls its origin from equation 3. Therefore further restrictions must be added to maintain at least a first order mismatch shaping functioning until the related SB comes out of its unstable situation [10], [11]. That is the reason why the proposed algorithm shown in figure 1 is partitioned into two part: Tree-structured part on the left side of its schematic where we can apply the earliest modification given on equation-4 for DBs and the last column on its right side (called Sub-DEM) with a different kind of algorithm.
As we noted above, using an unmodified SB in the last column can potentially lead to instability on the algorithm resulting in a very poor performance so here we try to find

other types of dynamic element matching schemes which can give better performance. However, using the DB's structure shown in figure 2 with equation-4 is surly comfort in order to maintain system stability for all of possible cases of Sub-DEM including first, second and third order mismatch-shaping algorithms shown by the authors in [5], [6], [10].

IV. Different cases of Sub-DEM blocks

In the proposed algorithm shown in figure 1, the left side is the same as the conventional TDEM with a modified switching block. Since the conventional TDEM algorithm cannot support a high performance mismatch-shaping within the last layers, the last column (shown on the right side of the figure) has to be realized with a different scheme.
Each group of the last blocks in DEM structure (called Sub-DEM) can be established by different ways. In practice, the Sub-DEM shown in the figure can be locally realized with one of the following schemes [12]:

- modified tree-structured algorithm,
- feed-back vector (or sorting) algorithm,
- data-weighted averaging algorithm (DWA),
- barrel-shifter structured algorithm,
- butterfly-shuffler structured algorithm,
- randomized dynamic element matching (RDEM).

The only two conditions are the compatibility with the TDEM part on its left side and mismatch-shaping in itself. Here, we explain the two first structures which are useful to construct a high performance DEM algorithm [9] and the third one which is the best algorithm to provide the first order lowpass or second order bandpass mismatch-shaping. The interested reader can also refer to reference [12].
First of all, the general form of mismatch-shaping function for such an algorithm is outlined. Then, the compatibility conditions have to be applied to any possible selection for Sub-DEM. As fully derived in [4], for a B-bit TDEM, the analog output of DAC ($Do_b(n)$) can be expressed as:

$$\begin{aligned} Do_B(n) &= (1+\overline{\alpha})v(n) + e(n) + \epsilon \\ \overline{\alpha} &= \frac{1}{2^B}\sum_{i=1}^{2^B}\alpha_i \quad , \quad \epsilon = \sum_{i=1}^{2^B}\epsilon_i \\ e(n) &= \Sigma_{k=1}^{B}\Sigma_{r=1}^{2^{B-k}}\Delta_{k,r}S_{k,r}(n) \\ \Delta_{k,r} &= \frac{1}{2^k}\sum_{i=(r-1)2^k+1}^{(r-1)2^k+2^{k-1}}(\alpha_i - \alpha_{i+2^{k-1}}) \end{aligned} \quad (5)$$

where the gain error $\overline{\alpha}$ only affects the loop gain and does not cause nonlinearity effect. The TDEM has a regenerative structure and all of the $S_{k,r}(n)$ must be vectors with a desired shape. It means that each vector has to be passed through a digital filter separately. However, here we must edit this equation to express it for the TDEM part of the proposed structure (left side only). Therefore, error term for all of the switching-blocks except which are laid in the last layer on the right, can be driven by only rewriting summation indices from $i = 2^b + 1$ to 2^B, as follows:

$$e_{TDEM}(n) = \Sigma_{k=b+1}^{B}\Sigma_{r=1}^{2^{B-k}} \ \Delta_{kr} \ s_{kr}(n) \quad (6)$$

If we express the error term from an equivalent block as a Sub-DEM block by replacing adequate indices in equation 5, for example number "$s = 1$", we obtain:

$$e_{Sub-DEM_1}(n) = \Sigma_{k=1}^{b}\Sigma_{r=1}^{2^{b-k}} \ \Delta_{kr} \ s_{kr}(n) \quad (7)$$

For the compatibly reason, any replaced Sub-DEM has to produce a similar error expression. Then, two important notes are the similar gain error and offset terms:

$$\begin{aligned} \Delta_s &= \frac{1}{2^b}\sum_{i=(r-1)2^k+1}^{(r-1)2^k+2^{k-1}}(\alpha_i - \alpha_{i+2^{k-1}}) \\ \epsilon_s &= \sum_{i=1}^{2^b}\epsilon_i \end{aligned} \quad (8)$$

Therefore, in order to complete the proposed algorithm, we must provide a sort of Sub-DEM block so that gives the equivalent offset and gain error terms and shapes other terms if there is any. In the following, three suitable case of such a Sub-DEM are presented.

A. Modified tree-structured algorithm

As a modified case of TDEM, we propose a new kind of switching block which allocates the preferred DAC cells in respond to each input code but without continuing tree structured topology which can also be called shortened tree-structured (STDEM). This type of switching blocks can be called *"ending-switching block" (ESB)*. In the most simple system, the ESB takes at least four cells as shown in figure 3.

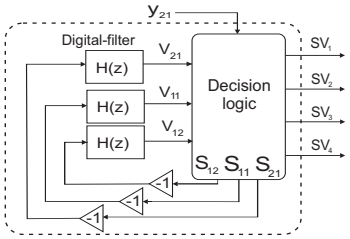


Fig. 3. General structure of an ESB used in STDEM algorithm.

Digital filters in the ESB can be a cascade of some (usually 2 or 3) integrators for lowpass and some resonators for bandpass applications. The decision logic is based on table-I, wherein the priority of any assignment for S_{ij}, $i, j \in \{1, 2\}$ is forced to regulate critical volume in digital filters in the related ESB. Threshold levels t_2 and t_1 are depended on the filter's order and structure which can be optimized by simulation or estimation. In order to fulfill number conservation rule and to be compatible with the rest of global TDEM, table-I must obey following expressions:

$$\begin{aligned} S_{11} &= sv_1 - sv_2 \ , \quad S_{21} = sv_1 + sv_2 - (sv_3 + sv_4) \\ S_{12} &= sv_3 - sv_4 \ , \quad y_{21} = sv_1 + sv_2 + sv_3 + sv_4 \end{aligned} \quad (9)$$

By this mean, there is no serious instability problem in switching blocks any more. This is because, $S_{kr}(n)$ accepts a desired non-zero value for any non zero input to the related SB. The most important error is $e(n)$ (equation 10)which must be reduced towards zero in the band of interest. Regarding $e(n)$'s equation, all of the $S_{kr}(n)$ must be a vector with a desired shape through different digital filters. For example, a 2-bit Sub-DEM needs 3 digital filters feeding by 3 shaped-sequences $\{S_{21}, S_{11}, S_{12}\}$, in both TDEM and STDEM algorithms. However, in STDEM, these sequences can almost freely accept nonzero values even if they receive even inputs. In fact, such a sequence has a much better mismatch-shaping performance than that of a conventional TDEM, which is realized by merging two first layers and using dynamic decision rules in its true table-I as well as employing equations 9.

TABLE I

DECISION LOGIC IN THE ESB

Y_{21}	Conditions on: V_{21}, V_{11}, V_{12}	$s_{21}s_{11}, s_{12}$	$sv1-4$
0	Don't-care	0, 0, 0	0000
1	$V_{21} \geq -t_2, V_{11} \geq t_1$	1, 1, 0	1000
"	$V_{21} \geq 0, V_{11} \geq 0, -t_1 \leq V_{12} < t_1$	1, 1, 0	1000
"	$V_{21} < t_2, V_{11} < -t_1$	1,-1, 0	0100
"	$V_{21} \geq 0, V_{11} < 0, -t_1 \leq V_{12} < t_1$	1,-1, 0	0100
"	$-t_1 \leq V_{11} < t_1, V_{12} \geq t_1$	-1, 0, 1	0010
"	$V_{21} < 0, -t_1 \leq V_{11} < t_1, V_{12} \geq 0$	-1, 0, 1	0010
"	$-t_1 \leq V_{11} < t_1, V_{12} < -t_1$	-1, 0,-1	0001
"	$V_{21} < 0, -t_1 \leq V_{11} < t_1, V_{12} < 0$	-1, 0,-1	0001
2	$V_{21} \geq t_2$	2, 0, 0	1100
"	$V_{21} < -t_2$	-2, 0, 0	0011
"	$-t_2 \leq V_{21} < t_2, V_{11} \geq 0, V_{12} \geq 0$	0, 1, 1	1010
"	$-t_2 \leq V_{21} < t_2, V_{11} \geq 0, V_{12} < 0$	0, 1,-1	1001
"	$-t_2 \leq V_{21} < t_2, V_{11} < 0, V_{12} \geq 0$	0,-1, 1	0110
"	$-t_2 \leq V_{21} < t_2, V_{11} < 0, V_{12} < 0$	0,-1,-1	0101
3	$-t_1 \leq V_{11} < t_1, V_{12} \geq t_1$	1, 0, 1	1110
"	$V_{21} \geq 0, -t_1 \leq V_{11} < t_1, V_{12} \geq 0$	1, 0, 1	1110
"	$-t_1 \leq V_{11} < t_1, V_{12} < -t_1$	1, 0,-1	1101
"	$V_{21} \geq 0, -t_1 \leq V_{11} < t_1, V_{12} < 0$	1, 0,-1	1101
"	$V_{11} \geq t_1$	-1, 1, 0	1011
"	$V_{21} < 0, V_{11} \geq 0, -t_1 \leq V_{12} < t_1$	-1, 1, 0	1011
"	$V_{11} < -t_1$	-1,-1, 0	0111
"	$V_{21} < 0, V_{11} < 0, -t_1 \leq V_{12} < t_1$	-1,-1, 0	0111
4	Don't-care	0, 0, 0	1111

B. Partially feed-back vector algorithm (SDEM)

Another suitable candidate for Sub-DEM is feedback vector algorithm which uses a local sorting scheme to arrange priority of DAC cells for new selection in each period. This algorithm has the best performance for mismatch-shaping but is very complex for a large number of DAC cells at the same times. Therefore, using the proposed algorithm let we benefit from good performance of SDEM partially in each Sub-DEM block with avoiding its complexity. Although, our proposed algorithm is general for replacing Sub-DEM blocks with a similar SDEM block, in the simplest case, the SDEM algorithm is used to map only 4 cells in each block as shown in figure 4. The error terms of such a mixed algorithm *(MDEM)* which uses a TDEM part followed by "*s*" time of the partial sorting algorithm can be expressed as:

$$Do_{MDEM}(n) = (1+\overline{\alpha})y(n) + e_{TDEM}(n) + e_{SDEM}(n) + \epsilon$$

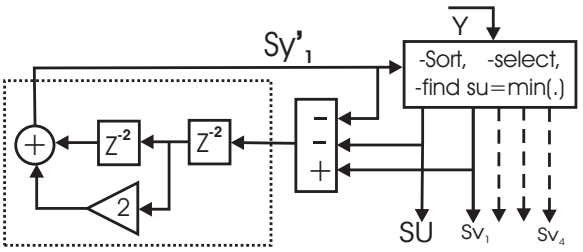


Fig. 4. Sub-DEM using a 4^{th} order bandpass SDEM algorithm partially

where:

$$\begin{aligned}
e_{TDEM}(n) &= \Sigma_{k=m+1}^{B}\Sigma_{r=1}^{2^{B-k}}\ \Delta_{kr}\ \ s_{kr}(n) \\
e_{SDEM}(n) &= \Sigma_{s=1}^{2^{B-m}}\ e_{SDEM_s}(n) \\
e_{SDEM_s}(n) &= \Sigma_{k=1}^{m}\ \Sigma_{r=1}^{2^{m-k}}\ \Delta_{s,k,r}\ \ sv_{s,k,r} \\
\Delta_{s,k,r} &= \frac{1}{2^k}\Sigma_{i=(j-1)2^m+(r-1)2^k+1}^{(j-1)2^m+(r-1)2^k+2^{k-1}}(\alpha_i - \alpha_{i+2^{k-1}}) \\
sv_{s,k,r} &= \Sigma_{i=(s-1)2^m+(r-1)2^k+1}^{(s-1)2^m+(r-1)2^k+2^{k-1}}\ (sv_i - sv_{i+2^{w-1}}) \\
\overline{\alpha} &= \frac{1}{M}\sum_{i=1}^{M}\alpha_i \quad , \quad \epsilon = \sum_{i=1}^{M}\epsilon_i
\end{aligned} \tag{10}$$

C. Modified Partitioned DWA

The conventional DWA algorithm, which is a first order low pass mismatch-shaping system, has a major drawback. It comes from appearing unwanted tones in the band of interest for a periodic input codes [8], [13], [14]. The partitioned structure of data-weighted averaging can relatively solve this drawback but not completely yet [9]. However, if we use a suitable SB based on equation 4 as a divider block in the TDEM part of the proposed algorithm, replacing DWA algorithm separately for each Sub-DEM block gives a good results without any tones in the band. This structure (called MP-DWA) is show in figure 5 for its simplest case. It uses two independent DWA and one modified SB. More details on this kind of dynamic element matching system are available in [12] applying to both lowpass and bandpass mismatch-shaping systems.

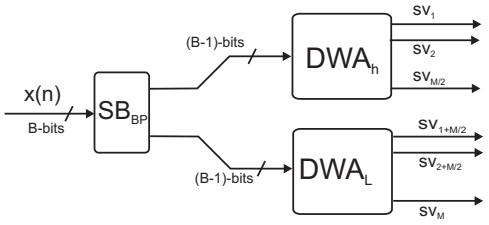


Fig. 5. MP-DWA Structure in the simplest case.

V. CIRCUIT DESIGN AND SIMULATION RESULTS

In today's CMOS technologies, circuits' mismatch standard deviation is in the order of a few tenth percents, (usually

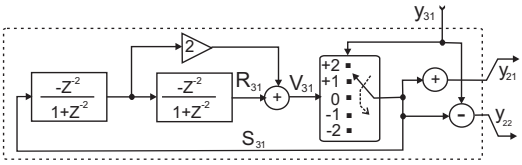


Fig. 6. Modified SB, used in all layers in STDEM but the last-one

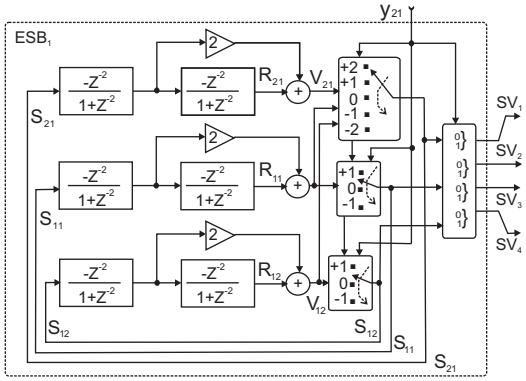


Fig. 7. Ending switching block schematic, used in the last layer of STDEM

$0.1\% \leq \delta I \leq 1\%$). This level of mismatch causes noise floor and unwanted tones to be increased in the band of interest. Without any correction, the worst-case standard deviation of the normalized DAC-output for a B-bit thermometric structure can be expressed as [2]:

$$\delta[DAC_{out,dB}] = 20log[\frac{\delta I}{2\sqrt{2^B+1}}] \qquad (11)$$

For example, supposing, $\delta I = 0.01$ and $B = 3$ results in a distortion of about $\approx -70dB$. In order to suppress this mismatch-noise in a high-resolution DSM (usually $DR \geq 96dB$ or 16 bit), using a first order noise shaping is not sufficient. Thus, a 2^d-order lowpass or a 4^{th}-order BP mismatch-shaping system will be needed regarding our applications[1].

Figure 6 shows a modified switching-block diagram for a 4^{th}-order BP-STDEM. It is completely realized in the digital domain. Since output of the special quantizer in such a modified SB's loop can accept a non-zero value for all of its non-zero inputs, the register's resolution requirement is quite modest, maximum five-bit at last resonator (V_{31}).

Figure 7 shows the present design of the 4^{th} order bandpass ESB wherein a sufficiently fluid group of decision rules is based on equations-9 and table-I. In order to estimate threshold levels t_1 and t_2, the critical volumes of digital filters' output values have to be considered. For the loop containing S_{21}, R_{21} and V_{21}, such a critical situation will start when the loop cannot be controlled for at least two periods ($S_{21} = 0$). If loop's integrators (or resonators) have non-zero values just before receiving such a tail of zero S_{21}, the second integrator can be overflowed in some periods. For example, when integrators' initial outputs are supposed to be 4 then, first one remains unchanged but the second stage output (here R_{21}) becomes grater than 8 and $V_{21} \geq 16$, while S_{21} is still zero. Therefore, the threshold value t_1 has to detect such an output growing tendency. This can simply be realized by regarding present value of V_{21} as in table-I. The estimated threshold level with this simple example is in the order of 16 and -16, respectively for positive and negative resonator's output. However, we are naturally interested in its minimum possible value to strictly control registers' values. Thus, in the same reasoning way but for one period of an unwanted output growing, a lowest threshold level estimated of about 8. In different practical simulations, these estimated values quietly results in proper mismatch shaping. The optimum value is obtained between 8 and 12, which are theoretically expected before. We can estimate the value of the second threshold level $t_{2,opt}$ in the same manner.

In order to compare with mixed structure constructed from local sorting Sub-DEM block, a similar segmentation must be used. Such a Sub-DEM block has been previously introduced in figure 4. Its register's tail is also low maximum 5 bit in the second resonator output (*SY'*).

The proposed algorithms using different kind of Sub-DEM block is simulated at system level with fixed register's precision. As discussed in the previous section, all registers' resolutions are limited to 5-bits plus a sign-bit. Figure 8 shows the SNR versus input level for a 8^{th} order bandpass DSM with a 3-bit quantizer [12]. A given mismatch error level of $\delta I = 0.01$ is properly corrected by a 4^{th} in both cases (MDEM and STDEM), which follows the ideal case. However, using 4^{th}-order conventional bandpass-TDEMs does not enhance the system's performance and its SNR may even stay below that of a pure system without any DEM.

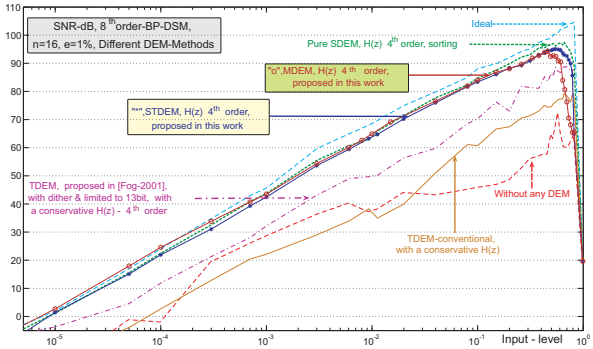


Fig. 8. Performance comparison between TDEM, MDEM and STDEM

The mentioned STDEM has been implemented in $CADENCE$ environment using $VERILOG$, then optimized by its $AMBIT$ software tools. Figure 9 shows a 6^{th} order bandpass modulator output spectrum for ideal, without any mismatch shaping and mismatch-shaping using a 4^{th}-order bandpass STDEM when DAC's cells have 0.9% mismatch [15]. The mismatch noise floor is decreased by ca. $35dB$ in the band of interest for $OSR = 100$. This circuit can be clocked with a maximum rate of $330MHz$ if it is implemented in a $0.35\mu m$-CMOS technology. A similar output spectrum can be

[1]Note that a fourth-order bandpass noise-shaping centered at $f_s/4$ is equivalent to that of a similar second order lowpass one

obtained for the case MDEM. However, its maximum clock rate is 50% lower than that of STDEM of about 150 MHz. In order to use the presented algorithms in a high-speed DSM, one period delay must be considered and compensated in system levels [12]. The proposed STDEM needs a $0.23\mu m^2$ area and contains about 3.000 gates as reported by AMBit in figure 9-c. In comparison, a similar MDEM algorithm needs $0.51\mu m^2$ area (9-b) and a similar pure SDEM needs $0.69\mu m^2$ area (9-a). While the performance of these three algorithms are close, we prefer the STDEM case for its more simplicity and its better hardware efficiency.

VI. Conclusion

In order to simplify DEM algorithm, a general manner was presented then three kind of realization schemes and the related circuits were presented for a high performance multibit delta-sigma modulator. The first case was a modified and shortened TDEM which is the most hardware efficient algorithm, the second one was a mixed of TDEM and SDEM algorithms which has a bite better performance but with more aria. The third one was a modified DWA algorithm which is suitable for first order mismatch-shaping application with no tones in the band. The related circuits use an analytically discussed and optimized decision logic for a 4^{th} bandpass mismatch-shaping, which were also well confirmed by system and transistor level simulations. All advantages of a conventional TDEM algorithm are maintained while its instability disadvantage is eliminated by a modified structure. Designed circuits, especially the shortened TDEM, need a moderate area and can be clocked faster than a comparable algorithm such as SDEM.

Acknowledgment

The authors would like to thank Prof. J. OKSMAN, Head of Department of Signal Processing and Electronic Systems at SUPELEC, and Prof. R. KIELBASA for their helpful suggestion and advice.

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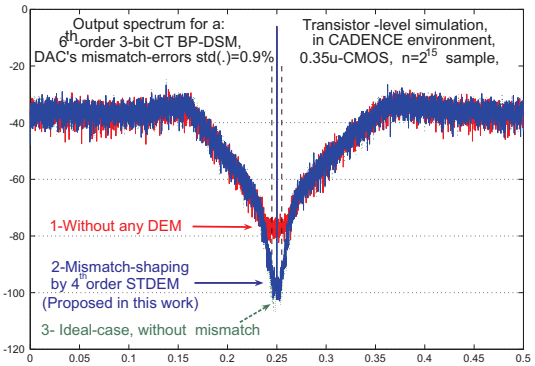


Fig. 9. Transistor-level simulation output spectrum for a 3-bit DSM using the simplified DEM algorithm proposed in this work.

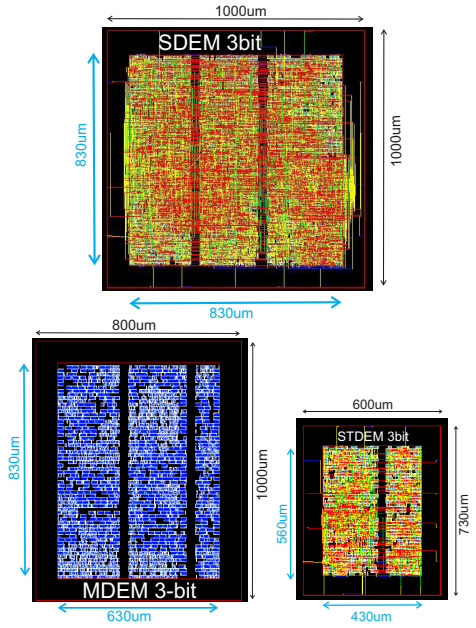


Fig. 10. Cheep aria need for a 4^{th} order bandpass mismatch-shaping system for a 3-bit DAC (Relatively): a) conventional SDEM, b) MDEM proposed in this work, c) STDEM proposed in this work.

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