A New Method to Synthesize and Optimize Band-Pass Delta-Sigma Modulators for Parallel Converters

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Abstract—**An analysis and synthesis method for continuous-time (CT) band-pass delta-sigma modulators, applicable in parallel converters is presented in this paper. This method makes the design of band-pass delta-sigma modulators possible in a wide range of central frequencies and high DAC+ADC delays. This method is also applicable for narrow-band delta-sigma converters in order to improve their performances.** *(Abstract)*

I. INTRODUCTION

Broad-band and wide-band applications require analog-to-digital converters with large bandwidth which creates limitations when using delta-sigma modulators.

In order to enlarge the bandwidth of a delta-sigma converter, the sampling clock frequency should be increased. However, the implementation of delta-sigma modulator is problematic due to the high frequency limitations [1]. Recently, the concept of parallel delta-sigma modulators has been introduced in several studies. A parallel converter uses M modulators working in parallel with each of them running at the same clock frequency [2]. This concept is a satisfactory solution since the signal bandwidth of the converter can be simply extended by adding more branches. In order to have a constant SNR ratio all over the bandwidth of the converter, each modulator should present similar Noise Transfer Function (NTF) in its own bandwidth.

The demand for high speed delta-sigma modulators can be satisfied by using CT methods. Generally it is feasible to clock CT delta-sigma modulators at much higher frequencies than discrete-time (DT) delta-sigma modulators. Furthermore, CT analog circuits are less demanding than their DT counterparts in terms of power consumption and chip area [3]. On the other hand, they are more sensitive to circuit non-idealities for a number of reasons. Some of which are inherent in CT delta-sigma such as loop delay and clock jitter noise. Moreover it is difficult to realize resonators with high-Q factors. Even though Q-enhancement circuits can be employed, the linearity of the resonator will be deteriorated. The resonance frequency of resonators is also subject to process variations and temperature fluctuations. Therefore automatic tuning circuits are required [4]. As a result, the performances of CT delta-sigma are not capable to match those of DT ones in terms of dynamic range and SNR but CT methods are the only known way to design wide-band converters[5].

This work is an extension of [6]. In section II, a method to transform a discrete-time modulator into its continuous-time equivalent is explained considering the stability issues. The section III illustrates the issues introduced by the topology which is presented in section II. In section IV the synthesis method of a band-pass modulator is explained associated with CT band-pass topologies and a new optimization method is presented. This method gives the capability to improve the modulator performance in a wide range of central frequencies.

II. CONTINUOUS-TIME MODULATOR DESIGN

The method used for the design and analysis of continuous-time delta-sigma is presented in this section. A CT delta-sigma can be completely designed in DT domain and synthesized from its DT counterpart [7].

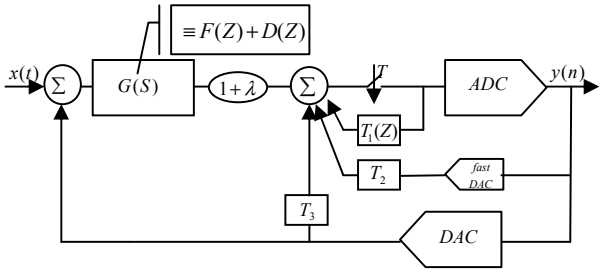


Fig. 1. Implementing a CT modulator with DAC delay

The delay introduced by both DAC and ADC, and the shape of DAC output signal are taken into account with this method. The DT designed filter ($F(Z)$) is transformed into CT domain ($G(s)$) by using (1) [6],

$$F(Z) = (1 - Z^{-1}) Z_T \left\{ L^{-1} \left[\frac{G(s)B(s)}{s} \right] \right\} - \sum_k a_k z^{-k} \qquad (1)$$

where L^{-1} denotes the inverse Laplace transform, Z_T is the z-transform at sampling period (T_s) and $B(s)$ denotes delay and non-ideality part of DAC and ADC functionality. In this approach, we use standard tools available in symbolic calculation programs such as Laplace and z-transform [7].
We denote:

$$D(Z) = \sum_{k=1}^{n} a_k z^{-k} \qquad (2)$$

$D(Z)$ can be considered as additive feedback terms between the modulator output and the ADC input [6]. The order of $D(Z)$ depends on the ADC+DAC delay and is equal to its

integer part plus one [7]. As it is shown in Fig. 1, due to the DAC delay, only $a_n z^{-n}$,which is the last term of $D(Z)$, can be realized by feedback 3 (T_3). An analog feedback ($T_1(Z)$) must be introduced to realize the first term of $D(Z)$ due to the analog-to-digital conversion time which is usually more than one sampling period [6]. The other terms can be realized either by an analog switched filter or by a fast DAC (T_2).

CT topologies are sensitive to analog parameters. Large mismatches in analog parameters may leads to performance degradation or even instability. We propose to analyze stability using the modulus margin. Employing the modulus margin has a main advantage. Modulus margin is a number which can be a comprehensible reference to compare different circuits' stability and sensitivity. Therefore, the modulus margin should be as great as it is possible.

Classical analysis stability methods use a virtual multiplicative coefficient (1+λ) in the loop. Modulus, gain and phase margin indicators correspond to different geometrical terms, characterizing the distance between the Nyquist plot of the open-loop and the critical point $[-1, j_0]$. As it is shown in Fig. 2, the modulus margin (Δz) is defined as the radius of the circle centered in $[-1, j_0]$ and tangent to the Nyquist plot of the filter [8].

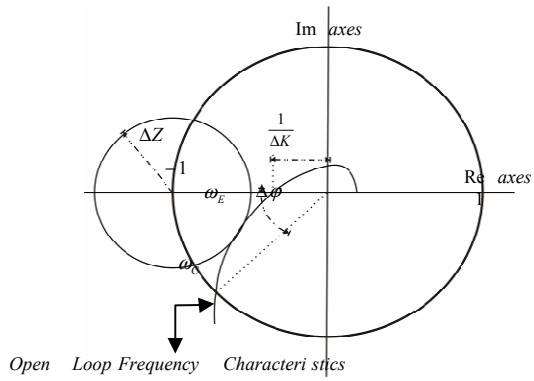


Fig. 2. Modulus (ΔZ), gain (ΔK) and phase ($\Delta\varphi$) margins for a open loop frequency characteristics

The definition of the vector connecting the critical point, with the Nyquist plot, results in:

$$\Delta z = \min\{|1 + NTF(j\omega)|\} = \min\left\{\left|s^{-1}(j\omega)\right|\right\} \Rightarrow$$
$$\Delta z = \left(\max\left\{\left|s(j\omega)\right|\right\}\right)^{-1} = \left(\left\|s(j\omega)\right\|_{\infty}\right)^{-1} \quad (3)$$

In another word the modulus margin is equal to the inverse of the modulus of the sensitivity function $s(jw)$ [8]. So modulus margin covers the gain and phase margins information.

It is preferable to be as little sensitive as possible to analog parameters. This margin is substantial and is counted as one of the most important parameters in the design of CT modulators.

The modulus margin, obtained by this method, depends on the modulator central frequency as is explained in section IV. Its maximal value is reached when the modulator central frequency (f_0), is equal to $f_s/4$ where f_s is the sampling frequency of modulator.

III. Dealing With Centeral Frequencies Other Than $f_s/4$

The principle of parallel wide-band converters is based on dividing the wide-band input signal into narrow-band parts [2]. Each part is digitalized by a branch. If the NTF of each branch's converter is not similar to the others, the global response of parallel structure will be disordered. Hence, a parallel structure, particularly the frequency band decomposition one, requires a cellule of converter in each branch which presents the same performance whatever the central frequency [2]. The model presented in Fig.1 is not suitable for this demand. Fig. 3 shows the NTF of a three resonators delta-sigma modulator designed in [7] using the proposed model in Fig.1 as a converter cellule for a frequency band decomposition parallel A/D.

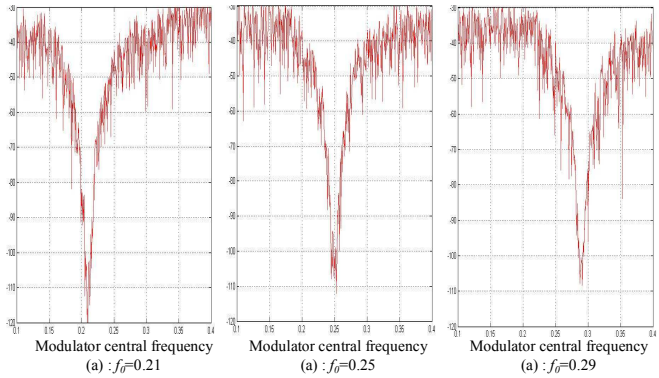


Fig. 3. DSP of output's noise versus central frequency for the topology of Fig. 1

The NTF change is due to feedback 1. In another word feedback 1 at the input of ADC, between output and input of the sample and hold function, produces resolution loss.

In order to understand the resolution loss, using linear model of sampler [7], the output signal of the global topology of Fig. 1 has been calculated as follow:

$$y(Z) = \underbrace{\frac{1-T_1(Z)}{1+F(Z)}}_{NTF} b(Z) + \underbrace{\frac{F(Z)+D(Z)}{1+F(Z)}}_{STF} x(Z) \quad (4)$$

The NTF of an ideal modulator (DAC+ADC delay =0) is equal to $\frac{1}{1+F(Z)}$. In this case the NTF is multiplied by $1-T_1(Z)$. $\|1-T_1(Z)\|$ at f_0 gives an estimation of the SNR variation. To show the influence of this term on the converter's performance $\|1-T_1(Z)\|$ is calculated for this three resonator delta-sigma modulator. The results are shown in Fig. 4. In general there is a progressive loss resolution when, central frequencies increases. Inversely, it can be noticed that in the special case in which the DAC delay is between $1T_s$ and $2T_s$ for the central frequencies lower than $0.25 f_s$, the performance is improved.

Furthermore feedback 1 leads to another kind of problem. Realizing feedback 1 is feasible with switched-capacitor or switched-current techniques which may limit the speed of the

modulator. Consequently, realizing this analog feedback may become the bottleneck of this topology.

It is now clear that the performance of this modulator, particularly its SNR, depends on the modulator central frequency due to the feedback 1. While approximately, the SNR is almost independent of DAC delay in each delay period. Taking these reasons in consideration, the proposed solution is to eliminate the feedback 1(Fig.5). Consequently the NTF will be no more depended on the central frequency. On the other hand, it is also interesting to eliminate feedback 2 to reduce the cost and complexity of implementation.

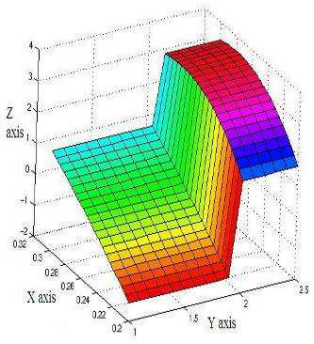


Fig. 4. $\|1-T_1(Z)\|_{dB}$ variation versus central frequency (X axis) and DAC delay(Y axis), the X axis range from $0.2f_s$ to $0.3f_s$, the Y axis range from $1T_s$ to $2.5T_s$.

IV. CONTINUOUS-TIME MODULATOR SYNTHESIS AND OPTIMIZATION METHOD

Once the global transfer function of the continuous-time filter ($G(s)$) is known [9], the next step is the synthesis of this transfer function. A sixth order delta-sigma modulator has been chosen in order to illustrate the process (Fig. 5).

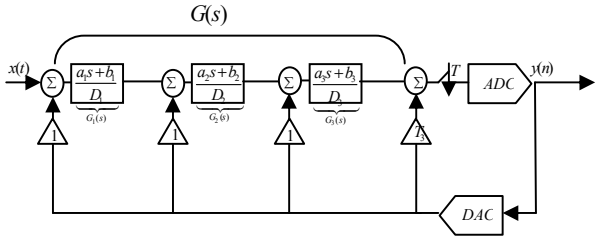


Fig. 5. Topology for a Continuous-time 6th order delta-sigma modulator.

The own resonators transfer functions ($G_k(s)$) can be deduced from $G(s)$ and can be expressed as:

$$\frac{N_k(s)}{D_k(s)} = \frac{a_k s + b_k}{s^2 + \frac{w_0}{p_k} s + {w_0}^2} \tag{5}$$

It has been supposed that $G(s) = N(s)/D(s)$. $D(s)$ can be fractionized as follow:

$$D(s) = D_1(s).D_2(s).D_3(s) \tag{6}$$

Equation 7 corresponds to the topology shown in Fig. 5.

$$G(s) = \underbrace{\frac{N_3(s)}{D_3(s)}}_{G_3(s)}\left(1+\underbrace{\frac{N_2(s)}{D_2(s)}}_{G_2(s)}\left(1+\underbrace{\frac{N_1(s)}{D_1(s)}}_{G_1(s)}\right)\right) \tag{7}$$

Due to eliminating T_1 and T_2, the NTF of proposed topology in Fig. 5 is not similar to those of Fig. 1. As a result, its NTF will not match the NTF expected from the delta-sigma modulator. In order to performances recovery, an optimization method is applied.

Due to the sample and hold function at the ADC input, the global transfer function of modulator (Fig.5) cannot be expressed in continuous-time. The proposed solution in this paper uses a transformation of CT modulator (Fig.5) to its DT equivalent. Afterwards the optimization criteria will be performed on DT transfer function. The optimization will be performed for the DAC delay between $1T_s$ and $2T_s$ due to the circuit instability by deleting T_1 and T_2 over $2T_s$.

In the present problem, there are an objective function and two constraints. The constraints are the nonlinear functions calculated by simulation, which are respectively SNR and modulus margin of filter. The objective function is a weight function achieved by combination of the two mentioned constraints. The goal of optimization is to maximize the objective function. So the problem can be put into the form:

$$\begin{cases} \text{constraint 1:modulus\_ma rgin} \geq (\text{modulus\_ma rgin})_{initial} \\ \text{constraint 2:} SNR \geq (SNR)_{initial} \\ \text{weight\_fun ction:} SNR + \text{modulus\_ma rgin} * 5 \\ \qquad + f_{NL}(\text{modulus\_ma rgin}) + f_{NL}(SNR) \end{cases} \tag{8}$$

The nonlinear functions employed in (8) have a major application. On defined interval, the constraints 1 and 2 are not convex. Respectively, the objective function is not convex. The nonlinear functions are defined so as to have a convex objective function. The function f ($f: R^n \to R$) is a convex set if its domain is convex and:

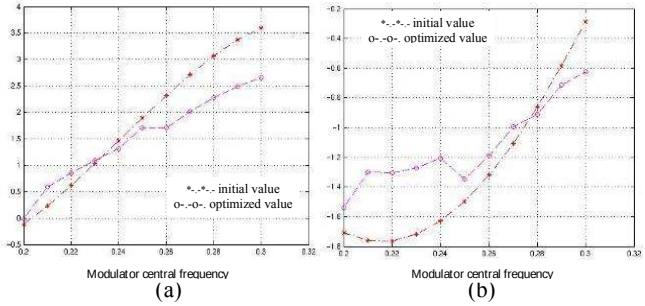
$$\begin{cases} f(\theta x + (1-\theta)y) \leq \theta f(x) + (1-\theta) f(y) \\ x, y \in \text{domain } f \text{ and } 0 \leq \theta \leq 1 \end{cases} \tag{9}$$

The nonlinear functions have been achieved by experience and are tested for different cases. Due to nonlinearity of the problem, application of nonlinear programs methods (NLP) is required [10].

The objective of this study is confirmation of this point that maximized optimization is achievable. In another word, when reaching the primary performance (initial performance achieved by using feedback 1 and 2), adjusting performance in all frequencies on set point is accessible to be used in parallel context.

To illustrate this process we consider, the sixth order band-pass delta-sigma modulator topology of Fig. 5 for a loop delay equal to $1.9T_s$ .As it is expected from the model specifications (Fig 5), performing optimization only on a_3 and b_3, brings out the required results. Fig. 6 shows the optimized values of a_3 and b_3. Comparing Fig.3 and Fig.7 shows the considerable improvement on NTF after optimization. As it is shown in Fig. 8, using this method has

two benefits, increasing modulus margin can be found as well as first SNR recovery. It should be mentioned that the results are related to the local optimum in the defined interval.



(a) (b)

Fig. 6. (a) a_3 values for initial and optimized topology, (b) b_3 values for initial and optimized topology; (DAC delay: 1.9 T_s)

These local optimums depend on the conditions which are forced by the constraints. So this method is compatible with design requirements and it is possible to find another local optimum with changing the constraints definition. Here, a little SNR loss has been preferred in order to increase 5significantly the modulus margin and as a result the stability.

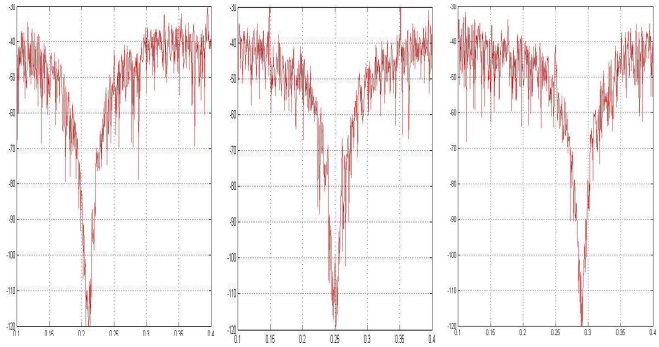
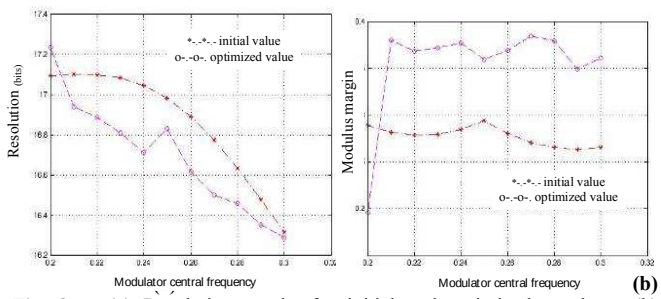


Fig. 7. DSP of output's noise of the optimized topology versus central frequency.

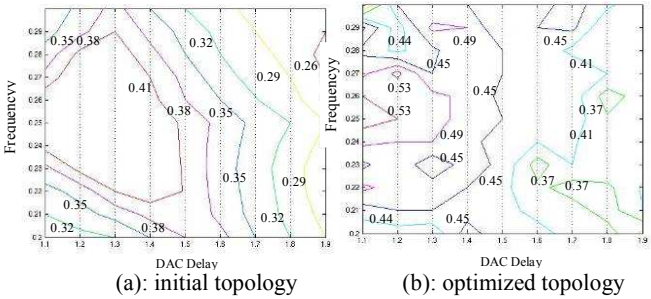
Fig.9 compares the modulus margin of the initial filter (Fig. 1) and that of the optimized filter (Fig. 5). This figure has been obtained by applying the contour command of MATLAB on modulus margin results versus DAC delay and f_0. Obviously, the modulus margin of the initial filter depends on f_0, particularly for the low delays of DAC. (Fig. 9.a.)



(b)

Fig. 8. (a) Resolution results for initial and optimized topology, (b) Modulus margin results for initial and optimized topology; (DAC delay: 1.9 T_s)

There is a great increase in term of modulus margin by performing the optimization. Furthermore, the modulus margin of the optimized topology becomes approximately independent of DAC delay and f_0 (Fig 7.b.).



(a): initial topology (b): optimized topology

Fig. 9. (a) Contour of modulus margin variation for the initial topology, (b) Contour of modulus margin variation for the optimized topology

V. CONCLUSION

In this paper, an optimization method for band-pass continuous-time delta-sigma modulators was briefly presented. The proposed optimization method has three major benefits. Firstly, by applying this method, we will be able to fix the performance of delta-sigma modulator all over its band, in the parallel context, or to find its best performance in the narrow band context. Making the modulators performances independent of DAC+ADC delay is the second benefit. As a result, the DAC+ADC between $1T_s$ and $2T_s$ allows applying dynamic element matching techniques, in the case of multi-bit modulators. The third benefit is to design a topology which is more and more insensitive to today's analog technologies tolerance thanks to modulus margin increase.

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