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low-consumption ΣΔ DAC for audio mobile applications

P. Benabes, R. Kielbasa

In this paper, we present a new Three-level D-to-A sigma delta converter for low consumption applications. The two one bit outputs of this converter can drive a loudspeaker directly without requiring passive components and with a sufficient audio quality. The global consumption is minimized by reducing the number of active states.

Introduction

Sigma delta modulators [1] are an attractive means of building D/A converters. They are usually composed of an interpolator, a single-bit or multi-bit sigma-delta digital modulator, a D/A converter, and an analog filter [2].

Multi-bit modulators are the most efficient ones as they usually do not present limit cycles, thus limiting non-linearities and spurious tones in the output signal. The crucial problem, however, is the need for a linear multi-bit D/A converter. Non-linearities can be reduced by the use of dynamic element matching algorithms associated with unitary sources [3]. Such algorithms increase the digital complexity, yet at the same time the analog part of the DAC requires a non negligible chip area.

Single-bit modulators are used for their intrinsic linearity. The one bit DAC can be replaced by a digital buffer which can provide two constant voltages. An H bridge can also be used, thus allowing to double the voltage applied to the loudspeaker. Passive components are usually introduced in order to filter the high-frequency one-bit signal components.

In the case of mobile applications, the price of external passive components is a limiting criterion. Furthermore, the consumption must be minimized in order to extend the life of the batteries. Applying a one bit signal is not a good solution because of the power consumption

in the passive elements, even in case of low audio signals. Most of the energy is dissipated in high frequency components.

The solution proposed in this paper is a three level modulator, [4] composed of 2 binary outputs and a new sigma delta algorithm, capable of reducing the output signal power.

Three level sigma-delta modulator

The principle of a three level second-order sigma-delta modulator is shown in Figure . The modulator is composed of two first-order integrators and a three level A/D converter.

The quantizer transfer function is :

$$\begin{cases} Q = 1 \text{ when } Y > L \Rightarrow Q_1 = 1,\ Q_{-1} = 0 \\ Q = -1 \text{ when } Y < -L \Rightarrow Q_1 = 0,\ Q_{-1} = 1 \\ Q = 0 \text{ elsewhere} \Rightarrow Q_1 = 0,\ Q_{-1} = 0 \end{cases} \quad (1)$$

The loudspeaker can be connected directly between the outputs Q_1 and Q_{-1} of the modulator.

Figure gives the output signal power dissipated in the parasitic resistive elements as a function of the input signal power. The output power *P* is defined as :

$$P = \frac{1}{N} \sum_{k=1}^{N} Q[k] \quad (2)$$

This curve was obtained from time-domain simulations of the topology shown above with an input equal to a sum of sine functions. We see that the output power decreases when the input signal amplitude decreases. However, the output power decreases at the beginning, it then then follows a flat path, and, finally, decreases again. We have been able to reduce power consumption to a certain extent, alas, not as much as we hoped for.

New modulator

In the solution presented above, middle-range signals induce output oscillations between -1 and +1, which, in turn, leads to transfers of energy at unaudible frequencies. We propose to use the sign of the input signal as a criterion : when the input signal is positive, the output cannot be negative and, inversely, when the input is negative, the output cannot be positive. A certain number of tests have resulted in the topology proposed in Figure .

The previous output Q (now Q_0) is used only as a feedback at the second integrator input. This feedback is required to ensure the stability of the loop.

The RAZ function is expressed as :

$$\begin{cases} Q = 0 \text{ when } Q_0 = 1 \text{ and } x < 0 \text{ and } Y < L2 \\ Q = 0 \text{ when } Q_0 = -1 \text{ and } x > 0 \text{ and } Y > -L2 \\ Q = Q_0 \text{ elsewhere} \end{cases} \quad (3)$$

This function means that the output cannot be +1 when the input is negative, except if signal Y is too large, and vice versa. The Y signal is defined as too large when its absolute value is larger than *L2*.

In the next simulation, we chose L = 3 and plotted the output signal power as a function of the input signal power. L_2 varied from 3 to 3.5. The system is very sensitive to the value of L2. For low L2 values, the system functions as a simple 3-level sigma delta modulator. If L2 is very large, consumption is reduced to the minimum.

Performance measurements

The design was coded in VHDL and implemented on a DE2 Altera board. The loudspeaker was connected through 6 74HC04 inverters, resulting in an 50Ω parasitic serial resistance.

Using an ampere meter, the supply current of the inverters (Table I) was measured for 4 configurations,

- single-bit modulator
- simple three-level modulator such as shown if Figure
- modified modulator with L=3 and L_2=124/32
- modified modulator with L=3 and L_2=∞

and 3 input signals: a zero signal, a very low level music signal, and a full scale music signal. The OSR is 256, resulting in a sampling frequency of about 11 MHz.

Compared to single-bit consumption, the lowest consumption configuration is the fourth one as it is divided by 250. However, this configuration creates spurious tones that are audible at low-level signals. Acoustic tests were performed for several audio levels. In terms of spurious tones, the most advantages configuration was obtained when L=3 and L_2=124/32.

Conclusion

This paper proposes a configurable D/A sigma delta converter adapted to low consumption applications with a direct connection to the loudspeaker. The lowest consumption configuration presents some audible spurious tones that can be minimized at the price of a consumption increase at low signals. However, these tones remain inaudible if the user's ear is at a certain distance from the loudspeaker (a mobile phone placed on a table, for example).

Acknowledgement

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Authors' afficiationsReferences

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Figure Captions

Figure 1: Encoder block diagram

Figure 2: Output signal power function of input signal power

Figure 3: New sigma delta topology

Figure 4: Output signal power function of input signal power

Figures

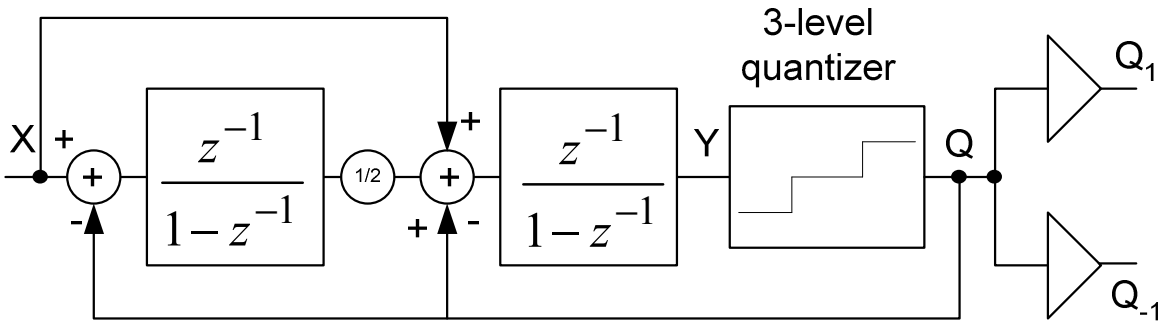


Figure 1

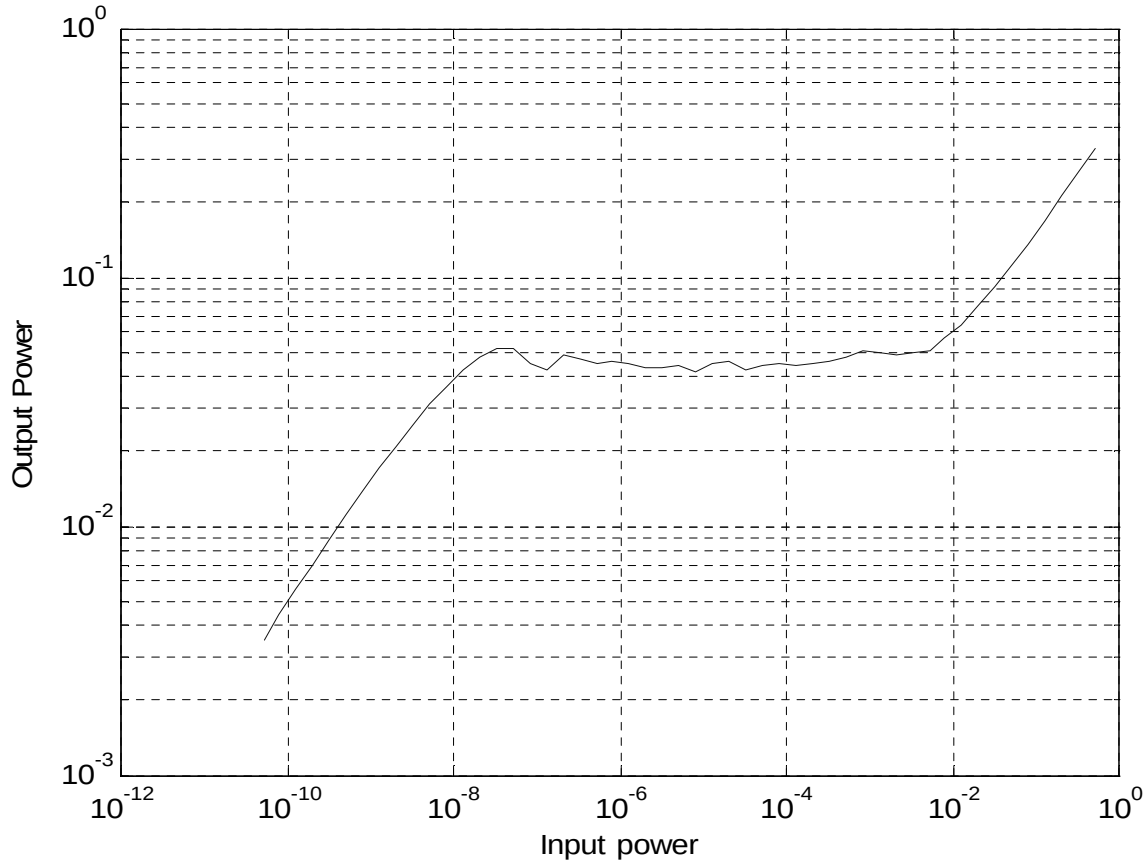


Figure 2:

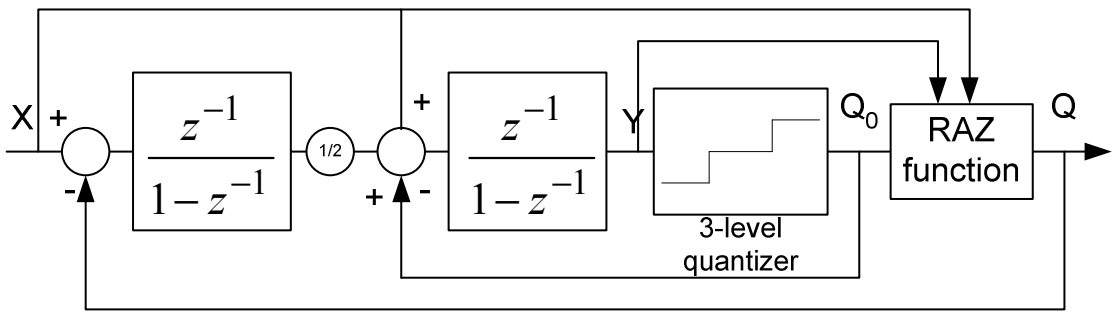


Figure 3:

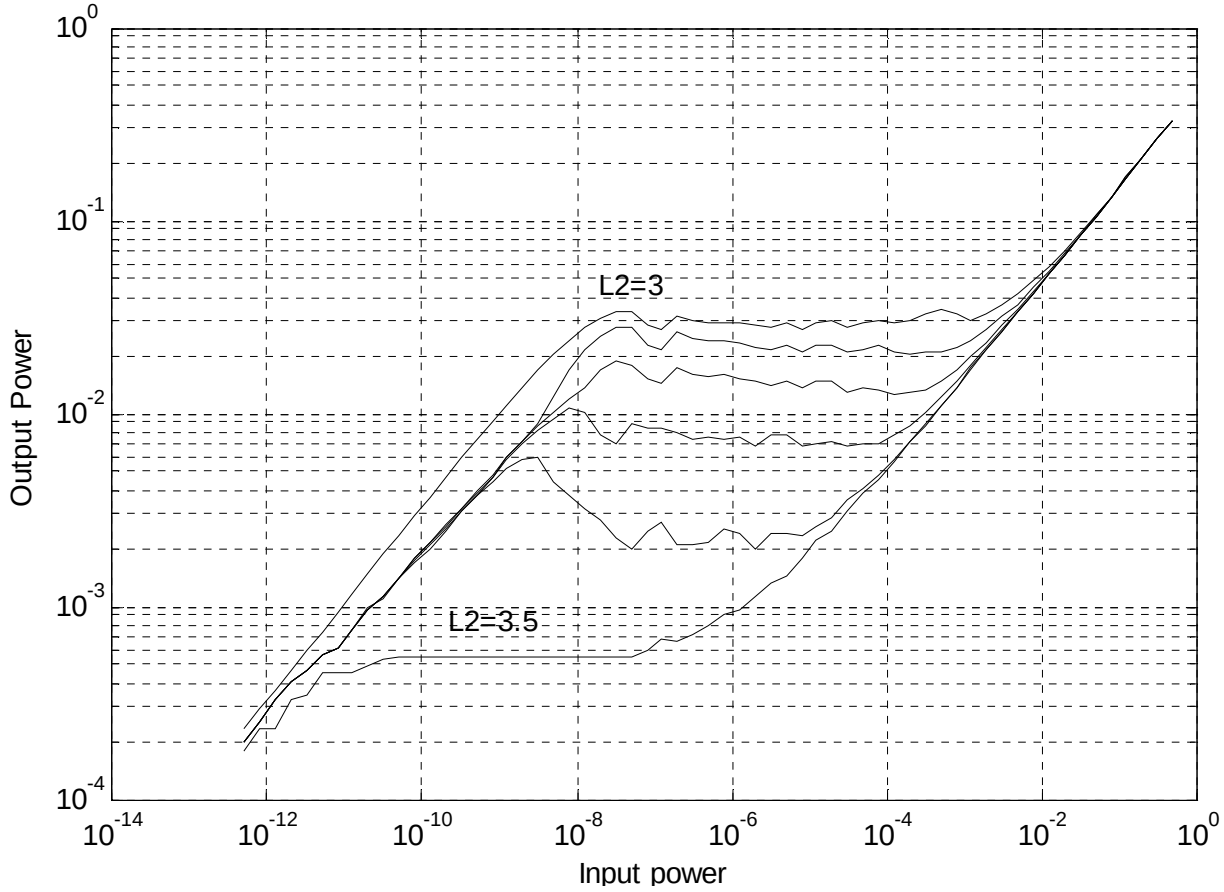

Output Power
Input power
L2=3
L2=3.5
10^0
10^-1
10^-2
10^-3
10^-4
10^-14
10^-12
10^-10
10^-8
10^-6
10^-4
10^-2
10^0

Figure 4:

Tables

Table 1: supply current for several configurations

	Null input	Very low input	Full scale input
Single bit	15.7 mA	15.7 mA	16 mA
3 level	4.6 mA	4.6 mA	5.5 mA
3 level $L = 3$, $L_2 = 124/32$	220 µA	300 µA	4.5 mA
3 level $L = 3$, $L_2 = \infty$	60 µA	200 µA	4.5 mA

Table 1: supply current for several configurations