A high-level modeling framework for the design and optimization of complex CT functions

Philippe BENABES, *Member*, *IEEE*, Catalin-Adrian TUGUI
Department of Signal Processing and Electronic Systems
SUPELEC
91192 GIF-SUR-YVETTE, FRANCE
philippe.benabes@supelec.fr

***Abstract*— Novel CMOS technologies are rapidly migrating towards the nanometer world. The design and optimization of complex analog circuits implying these processes is impracticable when using only transistor-level electronic design automation (EDA) tools. Efficient design methodologies including behavioral modeling are inevitable, but the high-level models should incorporate accurate circuit characteristics and technological limitations. One solution consists in using a refined top-down design process where the macro-models are extracted from the analog block elements (e.g. amplifiers, filters) implemented on specific technologies. These fast-simulating models can be used for the high-level simulation and optimization of the entire system. We propose in this paper a complete design methodology implying the above elements and the corresponding application framework based on the interface between MATLAB and CADENCE software tools. SIMULINK and VHDL-AMS are used for the high-level system modeling. A continuous-time (CT) Sigma-Delta modulator application is presented.**

I. INTRODUCTION

The evolution of complex analog systems towards nanometer-scale CMOS processes along with the increasing development of systems-on-a-chip (SoCs) and systems-in-a-package (SiPs) including mixed analog and digital circuitry imposes the existence of efficient analog design methodologies which can balance the high-performance digital implementation and verification techniques. Top-down design paradigms are preferred in order to handle together the digital and the analog parts and to ensure performance optimization directly at system level [1].

In this context, the design techniques implying only transistor-level Spice-like simulations of large analog functions such as continuous-time (CT) Sigma-Delta modulators [2] are prohibitive. Automatic optimization possibilities for a whole system are very limited due to the huge computation times required by each optimization step. Analog behavioral modeling should be considered in order to reduce the overall system conception and verification effort.

Several high-level modeling approaches have been proposed [3] [4] [5], still the largest problem remains the small number of systematic methods to create good analog behavior which can be exploited at system level and the lack of efficient tools to automate the macro-model extraction process.

One solution consists in using a refined top-down analog design methodology where the macro-models of amplification functions (Op-amps, Transimpedances, Transconductances) are extracted from transistor-level implementations of circuit blocks, including analog imperfections and technology constraints. Many topics have to be characterized such as the gains, the DC and AC transfer functions, the input and output impedances (real or complex), and the nonlinearities. All these characterizations require simulations which can become very long if they are not automated. The simulations tools do not have very flexible automation possibilities. This is why we propose an application framework MATLAB/SIMULINK – CADENCE – VHDL-AMS where the models extraction process is automated and system exploration can be performed easily at any architectural level.

Section II covers the novel aspects of the design methodology and the modeling approach. In the third section we present the interface between MATLAB and CADENCE and the overall techniques used to get the circuits characteristics. In the fourth section we propose a conception example for a fast current-to-voltage converter used in a Sigma-Delta CT modulator. System level implementation results are also presented. Section V covers the conclusions of this work.

II. DESIGN METHODOLOGY AND MODELING TECHNIQUES

Top-down design methodologies are used for complex analog and mixed systems, allowing fast system level simulations and performance evaluation. Still, the system level results, even when optimized, are rapidly degrading at transistor level due to technological dispersion and analog imperfections. In order to overcome the inconvenient, we propose a refined design methodology (Figure 1). Starting from a theoretically validated system architecture, the circuit design and the specific technology implementation are done. Then a semi-automatic optimization process is performed on each transistor-level cell using the MATLAB-CADENCE application framework. Using the optimal performance solution (in terms of desired gains, supply, impedances, nonlinear behavior, etc.) a robust component macro-model is

extracted. It includes circuit topology characteristics and real analog functions. Using the macro-models, a high-level system modeling and optimization can be performed, resulting in architecture, circuits and transistor-level adjustments.

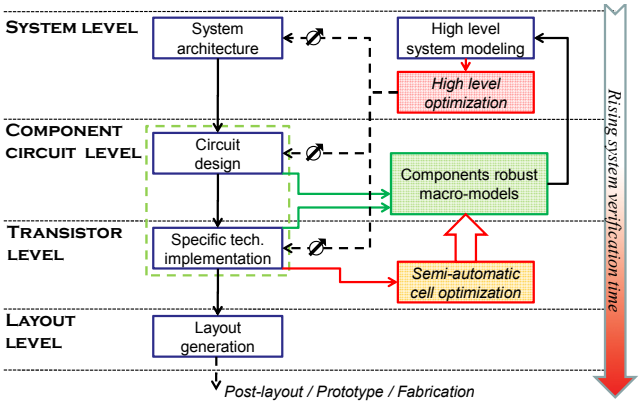

Figure 1: Refined top-down design methodology

An effective modeling technique is implemented. The fitting approach is combined with a constructive approach, where the unipolar and common-mode/differential behaviors are included. Three levels of models abstraction are presented as example in Figure 2. Including the parasitic effects and the imperfections at system level (Model 2), it is possible to directly optimize the system performance by taking into account the real components behavior.

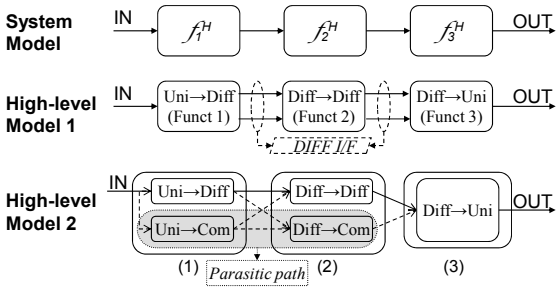

Figure 2: Abstraction levels for macro-models

III. ANALOG FUNCTIONS CHARACTERISTICS EXTRACTION

A. *Starting analog simulations from MATLAB*

In our case, MATLAB is used as a master tool and the analog simulator as a slave tool. The CADENCE integrated SPECTRE simulator was used. MATLAB functions were implemented in order to automatically create batch command files that will be read by the Open Command Environment for Analysis (OCEAN) interface tool. OCEAN starts all required transistor-level simulations. Then MATLAB can read the simulations results using the compiled functions delivered by CADENCE via their Virtuoso Multi-Mode Simulation (MMSIM) Spectre/RF toolbox.

Analog simulations can easily be started in a batch mode using the OCEAN tool. OCEAN is a text-based process that can be run from a UNIX shell. It can be used with any simulator integrated into the Virtuoso Analog Design Environment. OCEAN works in an existing simulation directory. So the first step is to create the schematic which has to be simulated and optimized. All the sizes of components should be parameterized with specific names which will be used as MATLAB variables in the framework. When the schematic is finished, the next step is to start the "analog environment" and create the simulation netlist. Once this step is completed, the Virtuoso environment can be closed and our MATLAB-CADENCE framework started.

B. *Performed analyses and macro-models extraction*

This tool is essentially dedicated to the optimization and macro-model extraction of CT functions such as amplifiers. The input and output quantities can be either currents or voltages. The interfaces can be unipolar or differential. In the rest of this presentation, we will consider a unipolar example with the input as a current and the output as a voltage, but all other cases can be treated. Four kinds of simulations can be performed: DC analysis, DC parametric analysis, AC analysis and transient analysis. All the analyses results are available as MATLAB variables, and can be synthetically grouped in two windows as presented in Figure 3 and Figure 4.

The MATLAB-CADENCE framework will completely automate the analog simulation process and extract s-models of the transfer functions, combine offsets, gains, nonlinearities and other user-defined criteria (e.g. normalization of the frequency band) and will synthesize the macro-model of the analog circuit as a SIMULINK block or VHDL-AMS behavioral architecture. A detailed description of the model extraction algorithms can be found in [6].

A more complex approach is used for the differential designs, where the common-mode/differential and normal input-output characteristics are studied.

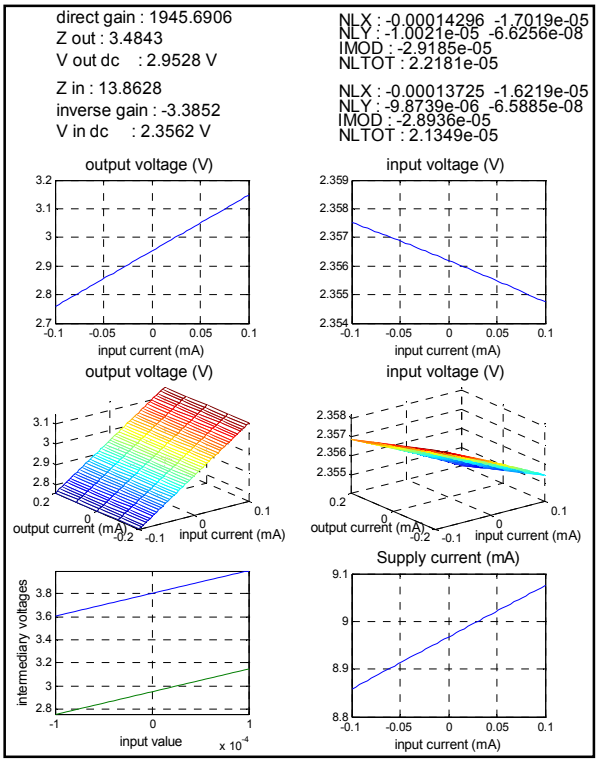

Figure 3: Macro-model DC parameters extraction

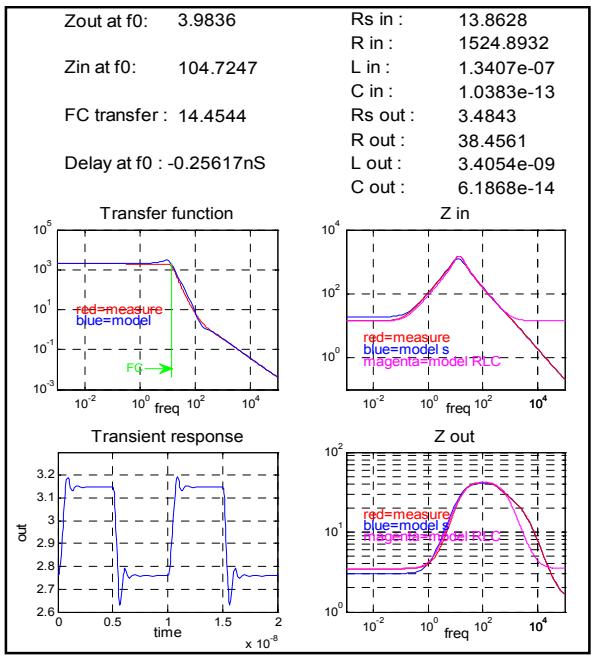

Figure 4: Macro-model AC/transient parameters extraction

IV. MACRO-MODELING A SIGMA-DELTA MODULATOR

The methodology will be applied to the design of the first stage of a sixth order CT Sigma-Delta modulator. The architecture of this modulator was published in [7]. As shown in Figure 5, its filter consists of three transconductance amplifiers (Gm1-Gm3), four transimpedance amplifiers (Z1 to Z4), three multi-output current mirrors (M1 to M3) and Lamb Wave Resonator (LWR) filters.

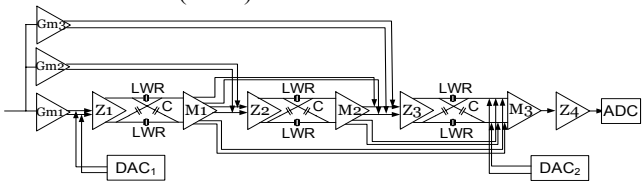

Figure 5: Sixth order Sigma-Delta modulator

The differential transimpedance amplifiers are composed with two single-ended transimpedance amplifiers. The schematic of each amplifier is given in Figure 6.

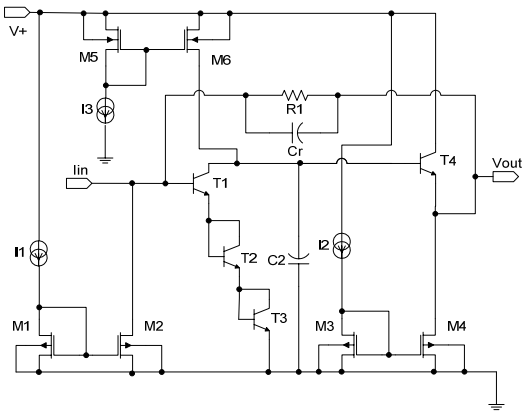

Figure 6: Transimpedance amplifier with real sources

Transistors T1, T4 and resistor R1 act as a current-controlled voltage source. Its gain is equal to R1. Transistors T2 and T3 are constant voltage sources. They help increase the base voltage of T1 and so the input offset voltage.

The current sources initial values can easily be found by simple DC considerations. Then a semi-automatic optimization process is performed using the MATLAB tool. The schematic is optimized with ideal current sources and afterwards the real sources are added and optimized also. The tool launches a parametric analysis on each transistor size and current source value. For the bipolar transistors the only parameter is their area. In the case of MOS transistors, optimal parameters would be their length (L) and geometric ratio (W/L). One performance parametric analysis result is shown as an example in Figure 7, but the tool gives one window per analyzed parameter. The total simulation time might take minutes or hours depending on the number of varied parameters, the schematic complexity, and the machine speed, but all is automatic and no human intervention is required.

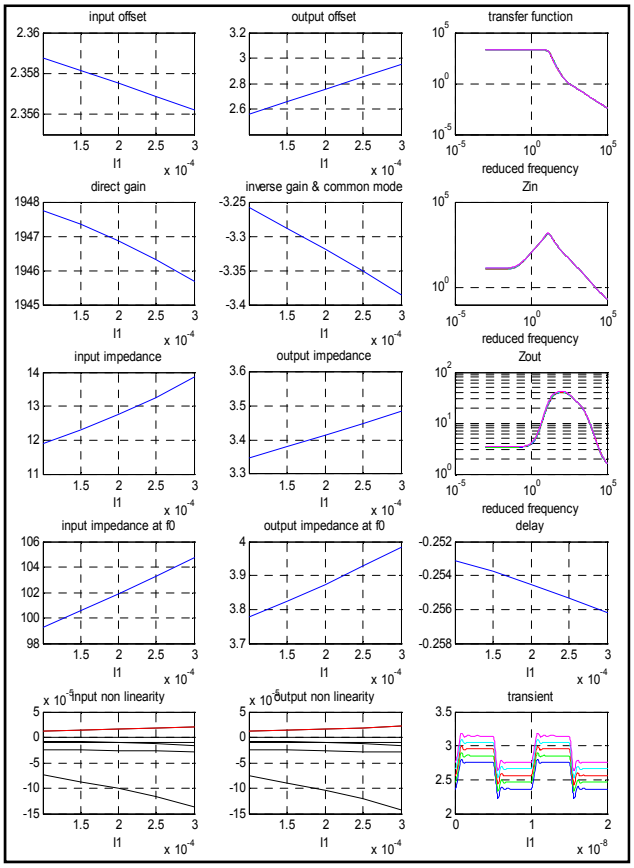

Figure 7 : Performance macro-parametric analysis

Once all the macro-parametric analyses were performed, the designer will deduce which parameter influences each performance characteristics and all components values can be usually found after 3 runs.

At the end of the optimization, one can extract the macro-model of the amplifier as a SIMULINK block (Figure 8) or VHDL-AMS module. The macro-model includes the direct and reverse transfer functions, the input and output

impedances, computed as minimum-order stable s-functions and all offsets. The nonlinear characteristics can be included on each output port of the model (in our case *Vout* and *Vin*) by using the computed nonlinearity coefficients $c_{ij}^{(r)}$:

$$V_{out} = V_{out\,0} + gI_{in} + Z_{out} I_{out} + c_{20} I_{in}^{2} + c_{11} I_{in} I_{out} + c_{02} I_{out}^{2} \quad (1)$$

$$V_{in} = V_{in\,0} + g^{r} I_{out} + Z_{in} I_{in} + c_{20}^{r} I_{out}^{2} + c_{11}^{r} I_{out} I_{in} + c_{02}^{r} I_{in}^{2} \quad (2)$$

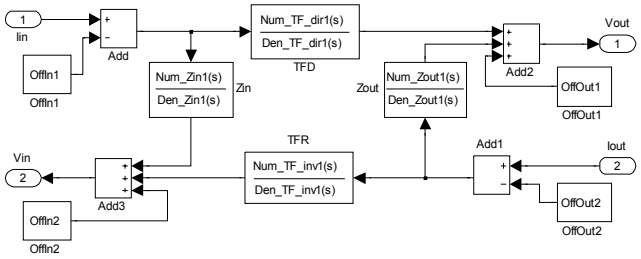

Figure 8 : Linear macro-model of the amplifier

The VHDL-AMS behavioral architecture of the amplifier is generated accordingly:

- Electrical terminals are used for the input and output ports:

  PORT (terminal Iin, Vout : electrical);

- S-functions are exported as vectors of real coefficients, e.g.

  CONSTANT Num_TF_dir1 : REAL_VECTOR := (23.141660, 13486.524207, -14874410.434859);
  CONSTANT Den_TF_dir1 : REAL_VECTOR := (1.000000, 177.429273, 7636.460716);

- Direct and reverse voltages and currents are defined as:

  QUANTITY v_d ACROSS i_d THROUGH ground to Iin;
  QUANTITY v_i ACROSS i_i THROUGH Vout to ground;

- The model behavior will use the Laplace formalism to find output signals starting from inputs and offsets, e.g.

  v_d == deltaIin'LTF(Num_TF_dir1, Den_TF_dir1) + deltaIout'LTF(Num_Zout1, Den_Zout1) + OffOut1;
  v_i == deltaIin'LTF(Num_Zin1, Den_Zin1) + deltaIout'LTF(Num_TF_inv1, Den_TF_inv1) + OffIn2;

When all amplifiers and LWR filters have been designed and extracted using the proposed methodology, the Sigma-Delta modulator can be implemented as a whole system in SIMULINK or VHDL-AMS based process. Each analog block in Figure 5 was replaced by a macro-model.

High-level implementations were conducted for second-order and third-order components models. MATLAB-SIMULINK and Dolphin Integration SMASH (for VHDL-AMS) were used as simulators. System level performance characteristics were evaluated in order to validate the methodology. As an example, the direct transfer function of the Sigma-Delta filter is compared in the case of the transistor-level implementation and the high-level one (Figure 9). The simulations results are coherent and more accurate when the maximum models orders increase. But orders>6 will not justify the plus-performance, while rising the system complexity. The macro-model simulation takes a few minutes while the transistor-level one requires hours.

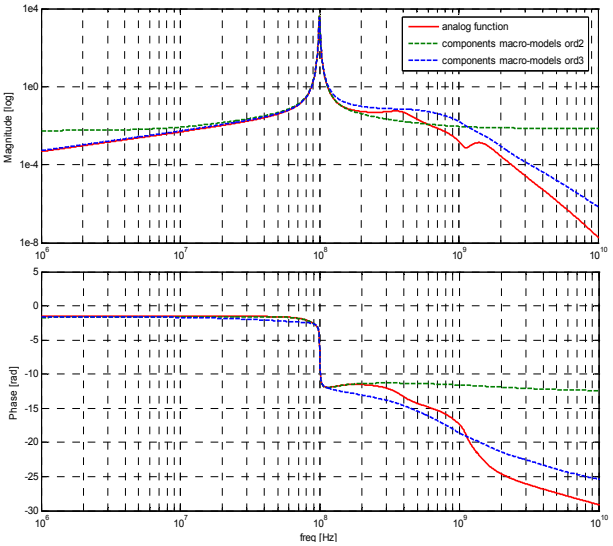

Figure 9 : Whole Sigma-Delta filter transfer function

V. CONCLUSIONS

A refined top-down design methodology for complex CT functions and the corresponding application framework employing the MATLAB/SIMULINK, CADENCE and VHDL-AMS tools were proposed. They can be used early in the conception stages in order to optimize the components sizes and for the extraction of effective components macro-models, in order to make a high-level implementation of the full system and accelerate simulations. The application can start automatically all kinds of analog simulations (DC, AC, parametric, transient), assure a semi-automatic optimization for the cells at transistor level and automate the macro-model extraction process. The proposed application framework and additional conception examples are available via the MathWorks website at [8].

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