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High-loop-delay 6th-order band-pass continuous-time sigma-delta modulators

M. Javidan, J. Juillard and P. Benabes

This paper focuses on the design of high loop delay modulators for parallel sigma-delta conversion. Parallel converters, allowing a global low oversampling ratio, consist of several bandpass modulators with adjacent central frequencies. To ensure the global performance, the noise transfer function of each modulator must be adjusted regarding its central frequency. In this thematic a new topology of 6th-order modulators based on weighted-feedforward techniques is developed. This topology offers an adequate control of the noise transfer function at each central frequency by simple means. Additive signal paths are moreover proposed to obtain an auto-filtering signal transfer function. An optimization method is also developed to calculate the optimized coefficients of the modulators at different central frequencies. The main concerns are improving the stability and reducing the sensitivity of the continuous-time circuit to analog imperfections. This is essential for parallel conversion since, in each channel, the modulator works at a central frequency which differs from the fourth of the sampling frequency. The performance of the optimized modulator is compared with its discrete-time counterpart with good argument.

1 Introduction

In broad band applications, many new approaches to achieve both high-resolution and large-band converters have been proposed. One is parallel sigma-delta ($\Sigma\Delta$) conversion, which performs the required signal-to-noise-ratio (SNR) in a wide frequency band without increasing the sample frequency (f_s) [1]. We explore, in the context of the VERSANUM project funded by the FRENCH ANR AFRU program, a novel technique to design parallel $\Sigma\Delta$ converters based on frequency-band-decomposition (FBD) technique [2]. The global oversampling ratio (OSR: defined as half the sample frequency divided by the converter bandwidth (Δf)) is decreased by putting in parallel high-order (≥ 4) modulators. Thus, each modulator passes one Mth of the signal frequency band when there are M modulators. In this project the normalized frequency band of interest is between $0.2f_s$ and $0.3f_s$ resulting in an equivalent OSR equal to 5. For example, with 8 modulators in parallel, the OSR of each modulator must be equal to 40, resulting in a global precision of about 12 bits. Higher precision can be theoretically reached by increasing the OSR of each modulator but the power consumption and the complexity of signal re-composition algorithms increase. Here an OSR equal to 64 is chosen resulting theoretically into 14 bits of resolution by 13 parallel modulators.

6th-order continuous-time (CT) band-pass single-stage $\Sigma\Delta$ modulators are good candidates in this thematic since they are high resolution converters, quite immune to coefficient errors and capable of working at high frequencies [3]. However, the sensitivity of the performance of CT circuits to analog imperfections (such as the excess loop delay) and the signal-dependent stability of high-order modulators are the main obstacles to overcome [4],[5],[6].

For high loop delay CT $\Sigma\Delta$ modulators, a methodology to calculate the CT loop filter ($G^*(s)$) through its discrete-time (DT) counterpart ($F(z)$) is

presented in [7]. Indeed there exist various methods and toolboxes to find the discrete-time transfer function corresponding to demands and the design of CT modulators may lean to this progress [8]. In [7] It is shown that $G^*(s)$ and $F(z)$ can be linked by:

$$F(z) = (1 - z^{-1})Z_T\{L^{-1}[\frac{G^*(s)B(s)}{s}]\} - \underbrace{\sum_{k=1}^{m} a_k z^{-k}}_{D(z)}, \tag{1}$$

in which L^{-1} denotes the inverse Laplace transform, $B(s)$ denotes the Laplace transform of the impulse response of the digital to analog converter (DAC) including the ADC delay and Z_T is the Z-transform with sampling period equal to T_s. $D(z)$ is introduced to ensure the existence of a solution for (1) i.e. finding an identification in z^{-k} term. It can be considered as additive feedback terms between the modulator output and the ADC input (Fig.1.a).

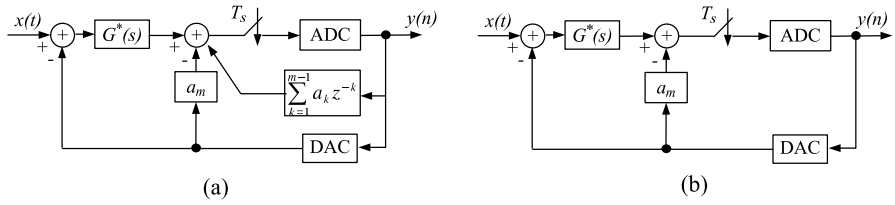

Figure 1: *Continuous-time modulator with DAC delay: a possible implementation of $D(z)$ (a) and the simplified topology (b).*

Because of practical issues widely discussed in [9], the implementation of the terms of $D(z)$ which have a delay less than the DAC delay faces several problems and in most of cases they are neglected (Fig.1.b). In (1) these terms correspond to $a_1z^{-1}, a_2z^{-2}, ...$ and $a_{m-1}z^{-(m-1)}$. As a result, the noise transfer function (NTF) and the signal transfer function (STF) of this design (Fig.1.b), called all over the paper the initial design, do not match the original DT modulator. This results in resolution loss and stability issues.

In recent studies, single-stage topologies are based on multi-feedback techniques [10], [11], [12], [13] inspired from [14]. The deteriorated performance of the initial design (because of the neglected terms of $D(Z)$) is

matched to the DT counterpart by tuning separately the pulses of two DACs in the feedback controlling the position of the poles of the NTF. The drawback is the sensitivity of the performance of high-order (≥ 4) modulators to nonlinearity of DACs. Although DAC linearity is achievable by correction methods such as dynamic element matching (DEM) [15], these methods result in increasing the size and the power consumption of the circuit as well as the loop delay. Moreover, at low OSR, DEM algorithm must be modified to prevent the occurrence of in-band signal-dependent tones in the modulator output spectrum [15]. The disadvantages of the linearization methods are doubled for multi-feedback topologies since two DACs are used.

Feedforward topologies with only one DAC are an alternative although their main inconvenient is a loop delay which is not a multiple of the clock period. We propose a new topology of 6th-order modulators based on weighted feedforward techniques with only one DAC. An optimisation method employing the pulses of the DAC together with the modifiable gain stages is also developed to control the position of the poles of the NTF. Extra signal paths are moreover added to obtain a filtering STF without missing the advantage of implicit anti-aliasing filtering of CT $\Sigma\Delta$ modulators. Indeed, in real applications, the input signal of the converter consists of both the desired frequency band and a wide spectrum interferer. Non-filtering STF results in reducing the dynamic range of the modulator.

In section II the proposed topology is described and the governing equations of the NTF and the STF are given. It is shown that the performance of the initial design, obtained through (1), is deteriorated for central frequencies other than $0.25f_s$ because of the absence of the neglected terms of $D(z)$. This design is optimized by the developed method in section III to recover the performance. In section IV a design example is given for f_s equal to 400 MHz. The scope of silicon implementation of the full system is also discussed. Finally conclusions are presented in section V.

2 Topology description

The proposed topology for 6th-order CT single-stage $\Sigma\Delta$ modulators is shown in Fig. 2. g_i is the feedforward coefficient, H_i is the resonator transfer function, k_i is the additional signal path coefficient and a_m, the last term of $D(z)$ in (1), compensates the excess loop delay.

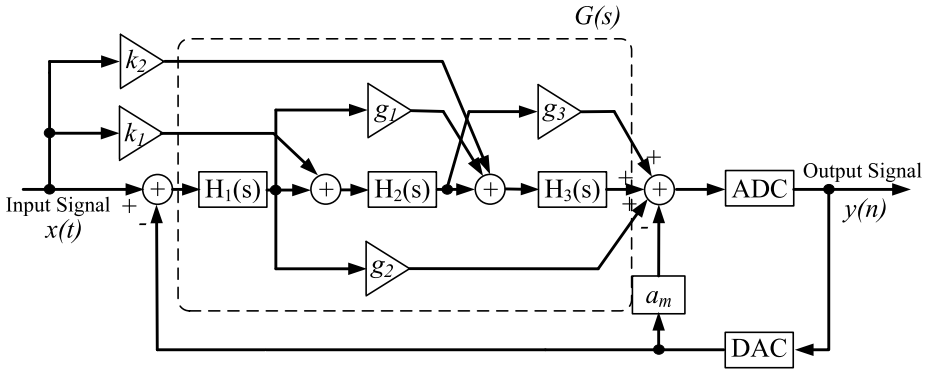

Figure 2: *Proposed filtering STF weighted-feedforward topology.*

The main differences between this topology and other feedforward topologies are g_1 which increases significantly the flexibility to control the poles of the NTF without modifying the zeros and k_i that modifies the STF without modifying the NTF.

2.1 Noise transfer function

The loop filter transfer function ($G(s)$) of the proposed topology illustrated in Fig. 2 is governed by:

$$G(s) = H_1(s)\left((g_3(s) + H_3(s))\,H_2(s) + g_2(s) + g_1(s)H_3(s)\right), \qquad (2)$$

in which each function can be replaced by the behavioral model of the corresponding analog component. In the ideal case $g_i(s)$ is simple gain and $H_i(s)$ is governed by $\frac{b_i}{s^2+\frac{\omega_{ri}}{Q_i}s+\omega_{ri}{}^2}$ (the transfer function of an ideal 2th-order resonator with a finite quality factor (Q)), in which $\omega_{ri} = 2\pi f_{ri}$ and f_{ri}

is the resonance frequency of the resonator, and b_i denotes the gain of the resonator.

For central frequencies (f_c) in the frequency band of interest ($0.2f_s < f_c < 0.3f_s$), loop delay between T_s and $2T_s$ and $Q = 75$, the analytically calculated parameters of $G(s)$ to fit $G^*(s)$ are shown in Fig. 3.

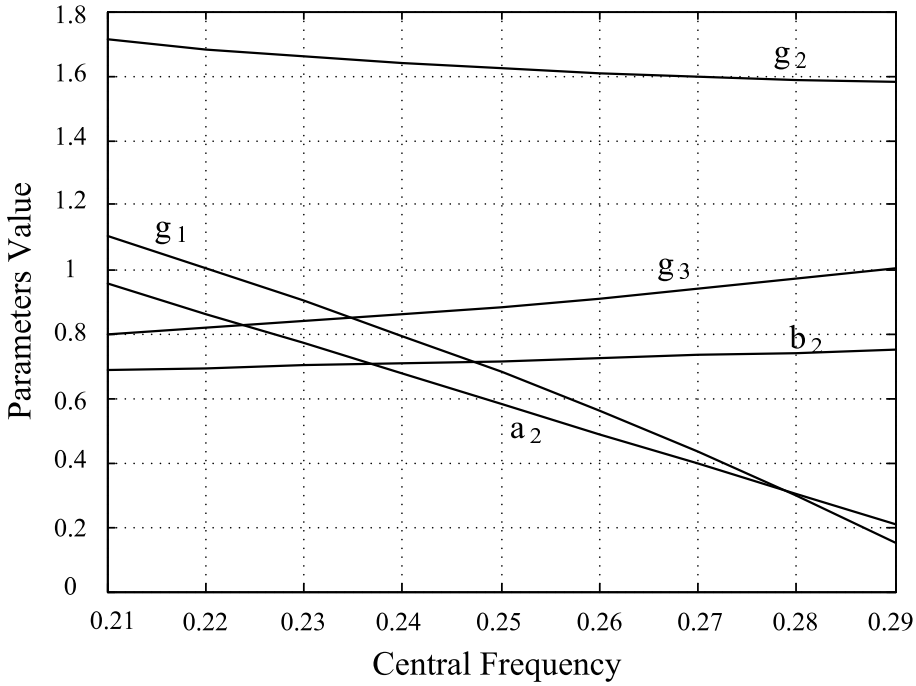

Figure 3: *Parameters of the initial design (Fig.1.b) to fit $G^*(s)$.*

b_1 and b_3 are chosen arbitrarily equal to 1 and 0.2 respectively since they are not independent degrees of freedom. a_2 is the last term of $D(z)$ governed by (3) for a loop delay between T_s and $2T_s$.

$$D(z) = a_1 z^{-1} + a_2 z^{-2}. \tag{3}$$

The variation of a_1, the non-implemented term of $D(z)$, is given in Table 1. a_1 is equal to zero for $f_c = 0.25f_s$ whatever the loop delay but it increases substantially when f_c moves away from $0.25f_s$. Fig. 4 compares the performance (the modulus margin and the bit resolution) of this initial design

Table 1: Variation of a_1 versus f_c for loop delay between T_s and $2T_s$.

f_c	$0.21f_s$	$0.23f_s$	$0.25f_s$	$0.27f_s$	$0.29f_s$
a_1	0.37	0.19	0	-0.19	-0.37

with that of the original DT modulator. The modulus margin (MM) is

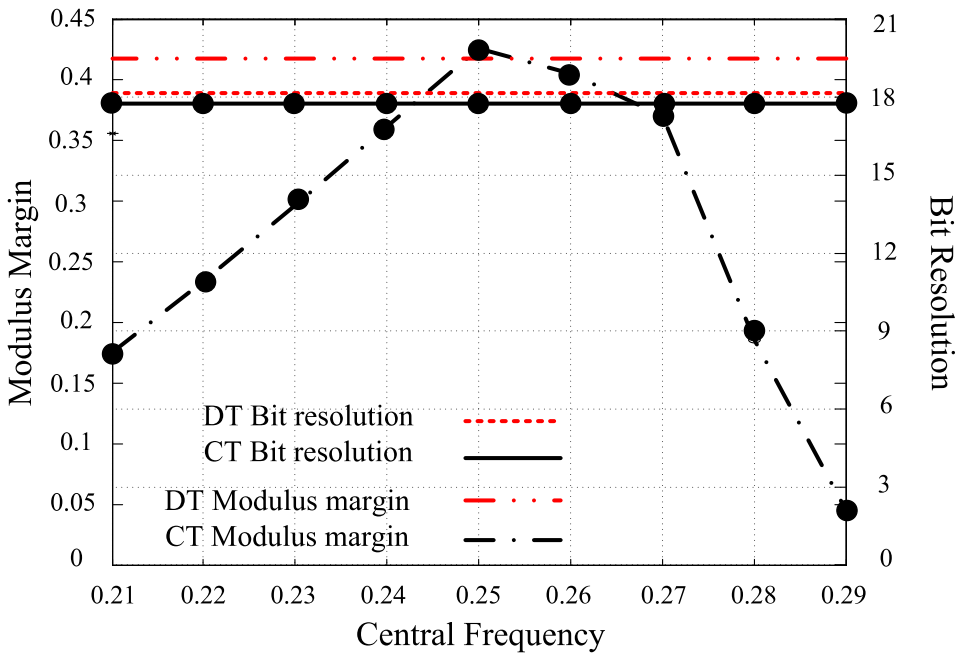

Figure 4: *Comparison between the performance of the initial design and the original DT modulator.*

a linear stability related performance criterion considered as a reference in order to compare different circuits stability and sensitivity. It characterizes the minimum distance between the Nyquist plot of the open-loop system and the critical point $[-1, j0]$. It is equal to the inverse of the modulus of the sensitivity function:

$$MM = min\left\{(1 + NTF(j\omega))\right\} = \left\{\left|S^{-1}(j\omega)\right|\right\}, \tag{4}$$

The interested reader can refer to [16]. As it is shown in Fig. 4, the resolution of the initial design corresponds to that of the DT modulator whereas the modulus margin does not. Indeed the absence of a_1 modifies the poles of the NTF while the zeros of the NTF are maintained fixed.

A small modulus margin indicates that the initial design is highly sensitive to imperfections for f_c other than $0.25f_s$. As it is mentioned in the introduction, in many studies an extra feedback is used to compensate the performance loss of the initial design while in section 3 it is shown that the provided degrees of freedom by the proposed topology are sufficient to recover the performance.

2.2 Signal transfer function

The expression of the STF cannot be directly governed in the s or the z domains since the input of the STF is CT while its output is DT. In order to calculate analytically the STF, the signal filter ($G_x(s)$) and the noise filter ($F_l(z)$) must be separated (Fig. 5). A sampler is placed after $G_x(s)$

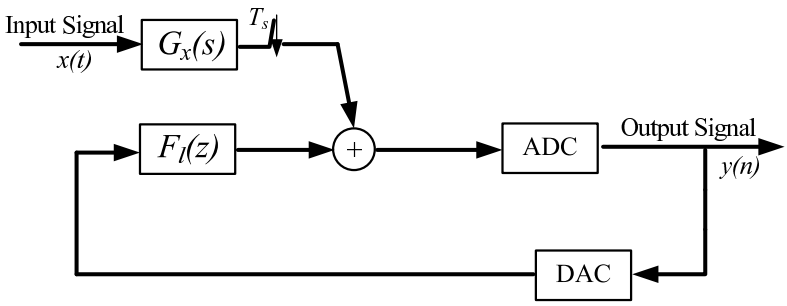

Figure 5: *System modifications to calculate the STF.*

to ensure the DT behavior of the model. The modifications are done in the sense that an input signal at pulsation ω gives, after a possible aliasing, an output component at pulsation $\omega - 2k\pi f_s$ where $-\pi f_s < \omega - 2k\pi f_s < \pi f_s$.

The expression of the STF can be then governed by:

$$STF(j\omega) = \frac{G_x(j\omega)}{1 - F_l(e^{j\omega T})}. \tag{5}$$

For the topology of Fig. 2, $G_x(s)$ is as follows:

$$G_x(s) = g_{x0}(s) + g_{x1}(s) + g_{x2}(s), \tag{6}$$

in which $g_{x0}(s)$ is the main signal path and $g_{x1}(s)$ and $g_{x2}(s)$ are the extra signal paths. The expression of $g_i(x)$ is governed by:

$$\begin{cases} g_{x0}(s) = H_1(s)\left(g_2 + g_1 H_3(s) + H_2(s)\left(g_3 + H_3(s)\right)\right), \\ g_{x1}(s) = k_1\left(H_2(s)\left(g_3 + H_3(s)\right)\right), \\ g_{x2}(s) = k_2 H_3(s). \end{cases} \tag{7}$$

For $f_c = 0.25 f_s$, Fig. 6 shows the STF when k_1 and k_2 are set to 0. The

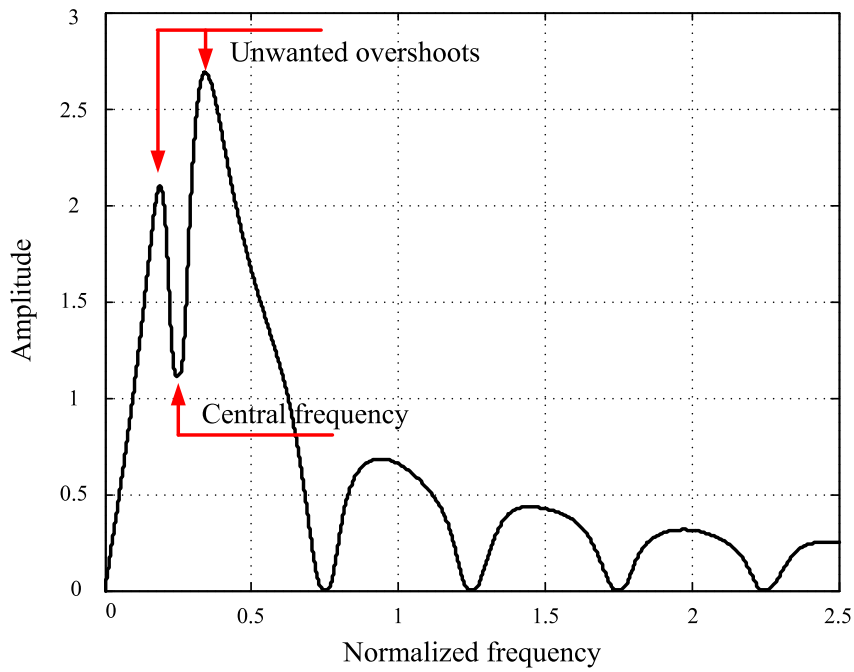

Figure 6: *STF for $k_1 = k_2 = 0$ at $f_c = 0.25 f_s$, the frequency axes is normalized by f_s.*

other parameters of the topology corresponds to the initial design (Fig. 3). The STF of feedforward topologies contains unwanted overshoots close to f_c. Indeed the design of feedforward $\Sigma\Delta$ modulators has traditionally been focused on increasing the order of the NTF to obtain a high SNR without destabilizing the modulator and most of conventional modulators containing only the main signal path ($g_{x0}(s)$) presents STF overshoots close to f_c. This results in decreasing the input dynamic range of the modulator. The proposed topology presents the advantage of STF shaping by tuning k_1 and k_2 to reduce the overshoots. The developed method to increase the modulus margin while maintaining the resolution and to shape the STF is described in the next section.

3 Optimisation method

As it was mentioned in section 2.1, the absence of a_1 modifies the poles of the NTF which may leads to performance degradation and even instability (Fig. 4). To answer the requirements of FBD converters (in which several modulators work at different central frequencies [2]), the stability margin at f_c other than $0.25f_s$ must be improved considering analog imperfections. In this regard the NTF and the STF are calculated by introducing in the loop filter transfer function (2) the system-level behavioral model of the analog components obtained from post-layout simulations. An optimisation method is developed to increase the modulus margin while maintaining the resolution and to shape the STF. This method can be used for other structures by calculating the proper NTF and STF.

3.1 NTF optimization

The vector of the modifiable parameters to optimize the modulus margin (MM) is:

$$\mu = [d,\ a_m,\ g_1,\ g_2,\ g_3,\ b_2]\,, \tag{8}$$

in which d corresponds to the loop delay and g_i and b_2 denote the DC gain of the feedforward coefficients and $H_2(s)$ respectively. It should be noted that b_1 and b_3 are not independent degrees of freedom. The starting point of the iterations, at each f_c, is the parameters of the initial design (Fig. 3). The optimization has to ensure a sufficient resolution (SNR) while maintaining certain immunity to analog mismatches (large modulus margin). We introduce the optimization criterion (κ) as :

$$\kappa = (1 - MM_{CT}) + \lambda_1 \left\| NB_{DT} - NB_{CT} \right\|^2 + \zeta, \tag{9}$$

in which NB_{DT} and NB_{CT} are the bit resolution of the original DT and the CT modulator respectively. MM_{CT} corresponds to the modulus margin of the CT modulator. Theoretically the modulus margin cannot exceed one. ζ is a regularization term given by:

$$\zeta = \lambda_2 \sum_i \frac{\partial((1 - MM_{CT}) + \lambda_1 \left\| NB_{DT} - NB_{CT} \right\|^2)}{\partial \mu_i}. \tag{10}$$

Although the exact partial derivatives cannot be calculated, a finite difference scheme is used to approximate ζ. Without ζ, the optimisation criterion (κ) has several local minima and a global minimum. Some of them are not reasonable answers since the derivative of κ versus some parameters of μ may be large. In such a case, there is a strong chance for performance degradation because of analog imperfections. It is important to study the global behavior of κ around the minima in function of modifiable parameters to obtain the reasonable ones. ζ is introduced to meet this goal. λ_1 and λ_2 are hyper parameters the values of which must be set by the user who must trade large modulus margin against resolution. Practical values are given

in the design example. A gridding method in association with the "Fmin search" function of MATLAB can be used to find the answers.

3.2 STF optimization

The second objective of the optimisation method consists in shaping the STF by adjusting the additive signal paths coefficients (k_1 and k_2). The proposed solution in this work (Fig. 7) consists in optimizing k_1 and k_2 to minimize the error between the ideal form and the real form of the STF. The error function to minimize in order to obtain a unity-gain STF can be

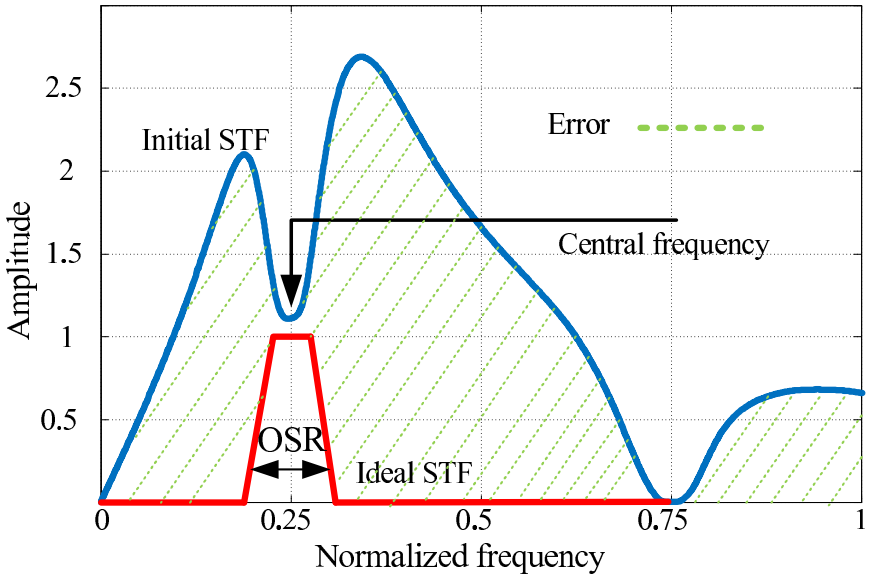

Figure 7: *principle of k_i optimization.*

governed by:

$$EF = \sum_{i=1}^{3} ef_i, \tag{11}$$

in which ef_1, ef_2 and ef_3 are given by:

$$\begin{cases} ef_1 = \int_{f_c-\frac{\Delta f}{2}}^{f_c+\frac{\Delta f}{2}} \left(\left\| 1 - \frac{G_x(j\omega)}{1-F_l(e^{j\omega})} \right\| \; df \right), \\ ef_2 = \int_{f_c+\frac{\Delta f}{2}}^{f_s} \left(\left\| \frac{G_x(j\omega)}{1-F_l(e^{j\omega})} \right\| \; df \right), \\ ef_3 = \int_{0}^{f_c-\frac{\Delta f}{2}} \left(\left\| \frac{G_x(j\omega)}{1-F_l(e^{j\omega})} \right\| \; df \right). \end{cases} \tag{12}$$

and Δf is equal to f_s/OSR. Once this objective is attained, the modulator is an auto-filtering system and it is less dependent on the input filter of the modulator to reduce interferer. Another possibility is to use a constrained optimization. In this case, the function to minimize is the maximum of the modulus of the STF out of band (Δf)). The constraint is the minimum of the modulus of the STF in band which must be higher than one. Both methods give almost identical results.

4 Design example

4.1 Behavioral models

In [2] it is shown that for broadband applications with low OSR, a large Q-factor (higher than 75) is necessary to achieve the required SNR. A large Q-factor can be obtained using piezo-electric resonators such as surface acoustic wave (SAW) [12] or lamb wave resonators (LWR) [17]. Their resonant frequency is also less sensitive to process and temperature variations. However they have their own disadvantages such as harmonic content and the anti-resonance frequency (Fig. 8.c). In [12], a differential structure using a compensation capacitance (C_c) is proposed to compensate the anti-resonance frequency. This structure and the corresponding electrical model are shown in Fig. 8, where x denotes the piezo-electric resonator and R_m, C_m and L_m are the mechanical resistance, capacitance and inductance, respectively. C_0 is the inherent static capacitance between the input and the output electrodes which produces the anti-resonance frequency. The anti-resonance is removed when $C_c = C_0$ although the performance of the modulator remains highly sensitive to mismatch between C_c and C_0. Also at low OSR the 3th and the 5th harmonics (modeled by R_{Hi}, C_{Hi} and L_{Hi}) can be interferer to the frequency band of interest because of the sampler in the $\Sigma\Delta$ modulator loop. On the other hand the real part of the input

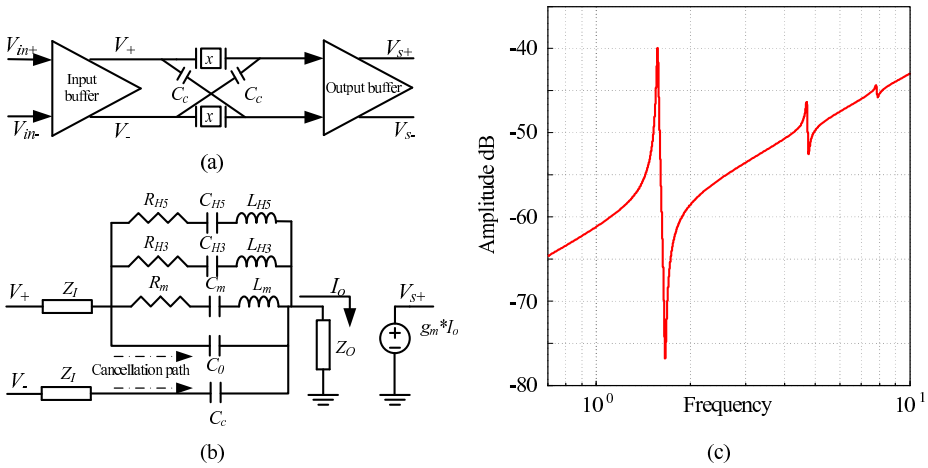

Figure 8: *(a): Electronic control circuit to remove the anti-resonance frequency. (b): Equivalent electrical model. (c) Frequency response of a typical LWR.*

(Z_I) and the output (Z_O) impedances of the buffers must be sufficiently small to maintain the Q-factor of the resonator. As a result the impedance of the cancellation path ($Z_I + \frac{1}{C_c s} + Z_O$) is low at high frequencies. The cancellation path demands a strong current for high frequency components of the resonator input signal. This current must be properly provided by the input buffer to ensure the differential functionality of the electronic control circuit. Moreover the linearity of Z_I and Z_O must be taken into account since they have a direct influence on the resonant frequency.

The mismatch between the nominal and the practical values of the DC gain of the gain stages (g_i and k_i) are also critical since it modifies the characteristics of the NTF and the STF. For this mean the gain stages are modeled by $\frac{\Gamma+\gamma}{1+\frac{s}{\omega_p}}$, where Γ denotes the DC gain, γ is the maximum error on the DC gain estimated through worst case simulations and ω_p corresponds to the first cut-off frequency pole.

The performance of the modulator is studied through SIMULINK simulation. The imperfections are modeled through the simulation of the ex-

tracted RC model of the analog components designed in AMS Bi-CMOS $0.35\mu m$ technology. The details of the electronic design and the fabrication are out of focus of this paper and will be detailed in a new paper.

4.2 Simulation results

Let us consider a 6th-order $\Sigma\Delta$ modulator with OSR = 64. The sample frequency (f_s) is equal to 400MHz. In the context of VERSANUM project we intend to employ LWRs performing a Q-factor equal to 75 [17]. Although a large Q-factor is considered, it is not a fundamental requirement of the proposed approach. The parameters of the equivalent model of the electronic control circuit (Fig. 8.b) are extracted from post-layout simulation presented in [18] containing the electrical response of the LWR [17]. Through the worst cases simulations, in AMS Bi-CMOS $0.35\mu m$ technology, the maximum error on C_c is up to 6%, the cut-off frequency of gain stages (ω_p) is down to $3f_s$, the real part of Z_I and Z_O is up to 40Ω and finally the error on the DC gain of the gain stages (γ) is up to 20%.

The parameters of the initial design and the optimized design are presented in Table 2. The initial design is unstable with analog imperfections while the stability is recovered for the optimized design with the same imperfections. However the resolution is reduced by 2-bits compared with the original DT modulator. The calculated values of k_i to achieve a filtering STF across the frequency band of interest ($0.2f_s < f_c < 0.3f_s$) is also shown in Fig. 9.a. For $f_c = 0.25f_s$, the optimized STF ($k_1 = 4.95, k_2 = -8$) is compared with the initial one ($k_1 \& k_2 = 0$). The amplitude axis is in logarithmic mode to prove that the additive paths have no influence on the implicit antialiasing filtering characteristic of the modulator.

The SNR of the optimized modulator and the output signal spectrum are shown in Fig. 10.a and Fig. 10.b respectively for $f_c = 0.25f_s$ considering the imperfections. To prove the reliability of this approach, the sensitivity of the

Table 2: The modifiable parameters, the modulus margin (MM) and the bit resolution (NB) before (Int.) and after (Opt.) optimisation

f_c	$0.21f_s$		$0.25f_s$		$0.29f_s$	
	Int.	Opt.	Int.	Opt.	Int.	Opt.
b_2	0.68	0.48	0.71	0.28	0.75	0.32
g_1	1.10	0.75	0.68	1.24	0.15	0.17
g_2	1.71	2.16	1.62	1.43	1.58	1.43
g_3	0.80	0.78	0.88	0.96	1.00	1.11
$d * T_s$	1.8	1.1	1.4	1.0	1.1	1.0
a_m	0.95	1.00	0.58	0.51	0.21	0.22
MM	–	0.58	–	0.62	–	0.61
NB	–	16.4	–	16.2	–	15.9

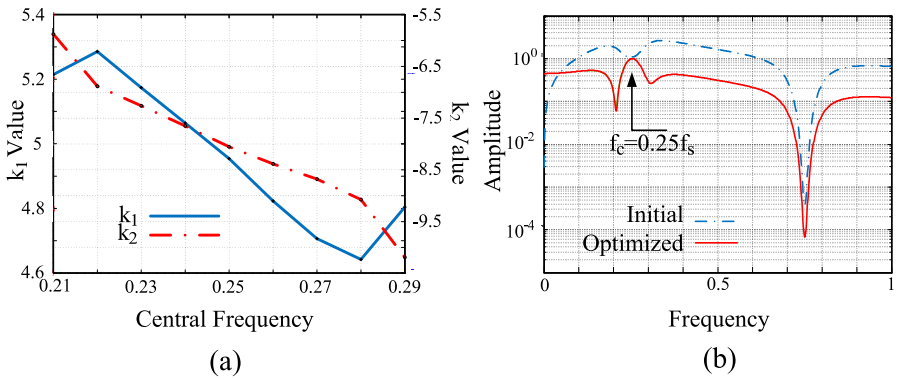

Figure 9: *(a): Calculated k_1 and k_2 across the frequency band of interest. (b): STF of the modulator before and after optimisation.*

optimized design to imperfections is compared to that of the initial design. The position of the critical poles of the NTF are compared in Fig. 11.a, for $f_c = 0.25f_s$ before and after the optimisation. As it is shown, some poles of the initial NTF lie outside the unit circle. So the modulator is unstable

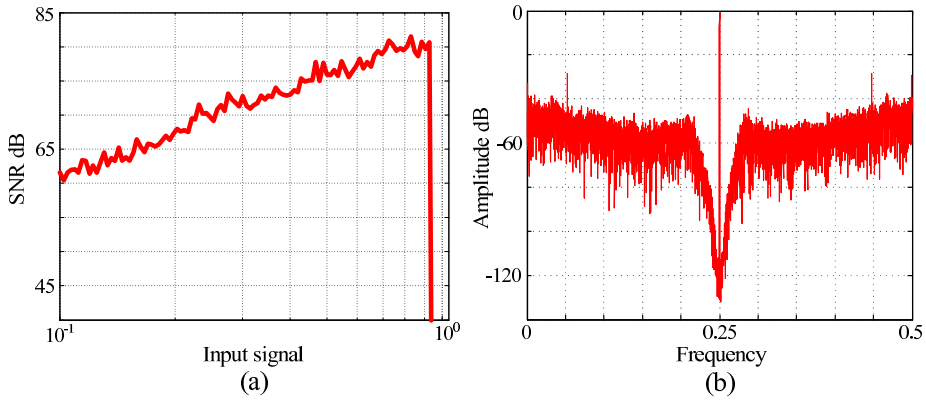

Figure 10: *(a): SNR of the optimized design. (b): Output signal spectrum of the optimized design.*

even for a null input signal. The distance between the NTF poles of the optimized design and the unit circle shows the reduction of the sensitivity to imperfections after optimisation. For $f_c = 0.25 f_s$, the influence of k_1 and k_2 variation on the STF is also shown in Fig. 11.c. As it is shown, the shape of the STF is not deeply modified even for 5% of error on k_1 and k_2. The sensitivity of the initial design to C_c errors is compared with that of the optimized design in Fig. 11.d. The initial modulator becomes unstable for an error on C_c larger than 2% while the optimized modulator is quite immune to C_c variation less than 6%. The influence of the variation of g_1 and g_3 on the modulus margin is also shown in Fig. 11.b. It should be noted that for a stable modulator, the variation of g_i and C_c have no influence on the resolution since they modify the position of the poles of the NTF and not the zeros. On the other side, the variation of the gain of the resonators modify the resolution since they change the gain of the feedforward path.

Here we have no intention to compare the proposed methodology with others since the results are obtained from a behavioral simulation. However it is shown that the proposed methodology is theoretically able to find the optimal parameters ensuring the performance of the modulator despite of

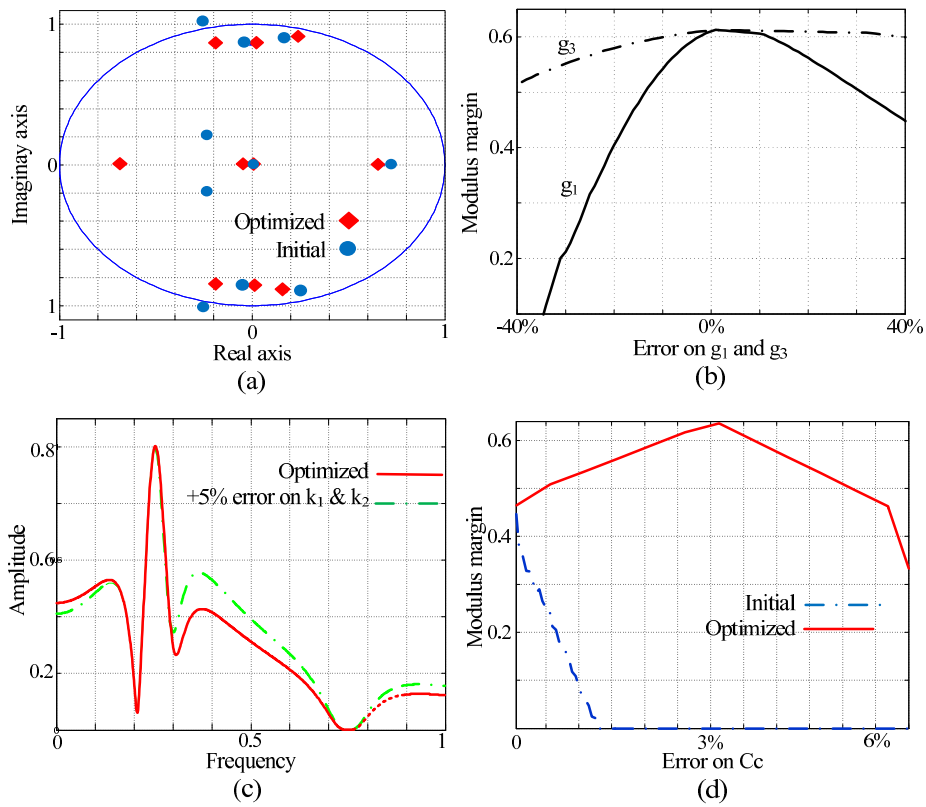

Figure 11: *(a): Position of the critical poles of the NTF of the optimized and the initial design. (b): Influence of g_1 and g_3 on the modulus margin of the optimized modulator. (c): Sensitivity of the STF to k_1 and k_2 variation. (d): Sensitivity of the optimized and the initial design to C_c errors.* .

imperfections.

4.3 Converter Implementation

Although the results are interesting in terms of stability and resolution, implementation issues must be overcome. The values of the optimized k_1 and k_2 are large. This complicates the design of the corresponding analog circuits. Moreover, the design of a tunable DAC delay is difficult since the linearity of the DAC is a critical parameter of high-order $\Sigma\Delta$ modulators.

The digital part of the project has been studied along the VERSANUM project [2]. It was shown that in a $0.35\mu m$ technology, the area of the digital part is around $0.8mm^2$ for each modulator, resulting in $6mm^2$ for 8 modulators. Using more recent technologies (0.65 nm), this area could be reduced $0.2mm^2$ for the whole converter. Several techniques, specially lamb wave resonators or BST filters (based on $Ba_xSr_{1-x}TiO3$ materials), are studied to implement the resonators. However all of them are off-chip components increasing the circuit size (upto $1mm^2$) and the sensitivity to the environment noise.

All modulators plus the digital part could be integrated in a single chip although the resonators are for the moment off-chip. This integration is in the scope of the European ARTEMOS project [19].

5 Conclusion

A new topology for 6th-order CT single-stage sigma-delta modulators based on weighted-feedforward techniques was proposed. This topology offers an adequate control of the NTF by feedforward coefficients. Another advantage of this topology is its filtering STF thanks to the additive signal paths. It was shown that for high loop delay structures, the required system modifications due to practical obstacles results in stability issues specially for f_c other than $0.25f_s$. Moreover it was shown that the CT modulator is highly sensitive to analog imperfections. A numerical optimisation method was developed to reduce the sensitivity to imperfections while maintaining the resolution. Major analog circuit imperfections such as the anti-resonance frequency of the piezo-electric resonators are modeled and are introduced in the optmisation algorithm. Then, the modifiable parameters of the modulator were determined through the optimisation method. The results of similations prove the reliability of this approach.

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References

[1] A. Eshraghi and T.S. Fiez, *A comparative analysis of parallel delta-sigma ADC architectures* , IEEE Transactions on Circuits and Systems I, vol. 51, issue 3, pp. 450-458, March 2004.

[2] P. Benabes, A. Beydoun and J. Oksman, *Extended frequency-band-decomposition sigma-delta A/D converter* , SpringerLink Journal on Analog Integrated Circuits and Signal Processing , vol. 61, issue 1, October 2009.

[3] C. Candy and G.C. Times, *Oversampling delta-sigma data converters : theory, design, and simulations*, Handbook , Wiley-IEEE Press, September 1991.

[4] K. Reddy and S. Pavan, *Fundamental limitations of continuous-time delta-sigma modulators due to clock jitter*, IEEE Transactions on Circuits and Systems I, vol. 54, issue 10, pp. 2184-2194, October 2007.

[5] O. Oliaei, *Design of continuous-time sigma-delta modulators with arbitrary feedback waveform*, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, vol. 50, issue 8, pp. 437-444, August 2003.

[6] G. Fischer and A.J. Davis, *Alternative topologies for sigma-delta modulators- A comparative study*, IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing , vol. 44, issue 10, pp. 789-797, October 1997.

[7] A. Yahia and P. Benabes, *Bandpass sigma-delta modulators synthesis with high loop delay*, IEEE International Conference on Circuits and Systems, vol. 1, pp. 344-347, May 2001.

[8] A. Hamoui and K.W. Martin, *High-order multibit modulators and pseudo data-weighted-averaging in low-oversampling $\Delta\Sigma$ ADCs for broad-band applications*, IEEE Transactions on Circuits and Systems I, vol. 51, pp. 72-85, January 2004.

[9] M. Javidan and P. Benabes, *A new method to synthesize and optimize band-pass delta-sigma modulators*, IEEE International Conference on Circuits and Systems and TAISA Conference, pp. 197-200, June 2008.

[10] N. Maghari, G.C. Temes and U. Moon, *Single-loop $\Sigma\Delta$ modulator with extended dynamic range*, IET Electronics Letters, vol.44, pp. 1452-1453, December 2008.

[11] J.A.E.P Van Engelen, R.J Van de Plassche, E. Stikvoort and A.G. Venes, *A sixth-order continuous-time bandpass sigma-delta modulator for digital radio IF*, IEEE Journal of Solid State Circuits, vol. 34, issue 12, pp. 1753-1764, December 1999.

[12] R. Yu and Y. Xu, *Band-pass sigma-delta modulator employing SAW resonator as loop filter*, IEEE Transactions on Circuits and Systems I, vol.54, issue 4, pp. 723-735, April 2007.

[13] A. Ashry and H. Aboushady, *Simple architecture for subsampling LC-based $\Sigma\Delta$ modulators*, IET Electronics Letters, vol.46, pp. 1263-1264, September 2010.

[14] J. A. Cherry and W. M. Snelgrove, *Excess Loop Delay in Continuous-Time Delta-Sigma Modulators*, IEEE Transactions on Circuits and Systems II, vol.46, issue 4, pp. 376-389, April 1999.

[15] N. Rakulijic and I. Galton, *Tree-structured DEM DACs with arbitrary numbers of levels*, IEEE Transactions on Circuits and Systems I, vol. 57, pp. 313-322, June 2009.

[16] C.S. Banyasz and L. Keviczky, *A new gap metric for robustness measure and regulator design* , 17th IEEE Mediterranean Conference on Control and Automation (MED '09) , Thessaloniki, Greece, June 2009.

[17] M. Desvergne, C. Bernier, P. Vincent, Y. Deval and J.B. Begueret, *Intermediate frequency lamb wave resonators and filters for RF receiver architectures* , IEEE International Conference on Electronics Circuits and Systems , vol. 10, issue 13, pp. 1045-1048, December 2006.

[18] M. Javidan and P. Benabes, *Design of electronic control circuit of piezo-electric resonators for $\Sigma\Delta$ modulator loop in AMS Bi-CMOS 0.35μm* , IEEE International Conference on Circuits and Systems and TAISA Conference , pp. 45-48, June 2010.

[19] http://www.artemos.eu