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Explicit analytical modeling of the low frequency a-Si:H/c-Si heterojunction capacitance: Analysis and application to silicon heterojunction solar cells

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We develop a fully analytical model in order to describe the temperature dependence of the low frequency capacitance of heterojunctions between hydrogenated amorphous silicon (a-Si:H) and crystalline silicon (c-Si). We demonstrate that the slope of the capacitance-temperature (*C-T*) curve is strongly enhanced if the c-Si surface is under strong inversion conditions compared to the usually assumed depletion layer capacitance. We have extended our analytical model to integrate a very thin undoped (i) a-Si:H layer at the interface and the finite thickness of the doped a-Si:H layer that are used in high efficiency solar cells for the passivation of interface defects and to limit short circuit current losses. Finally, using our calculations, we analyze experimental data on high efficiency silicon heterojunction solar cells. The transition from the strong inversion limited behavior to the depletion layer behavior is discussed in terms of band offsets, density of states in a-Si:H, and work function of the indium tin oxide (ITO) front electrode. In particular, it is evidenced that strong inversion conditions prevail at the c-Si surface at high temperatures down to 250 K, which can only be reproduced if the ITO work function is larger than 4.7 eV. © *2015 AIP Publishing LLC*.
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I. INTRODUCTION

Hydrogenated amorphous silicon/crystalline silicon (a-Si:H/c-Si) heterojunctions have drawn a lot of attention as promising candidates for solar cell fabrication due to low cost manufacturing, passivation properties of a-Si:H, and high electronic quality of c-Si. Several groups have obtained solar cell conversion efficiencies above 22%,[1–3] with a record at 25.6% achieved by Panasonic.[4] Recently, some attention has been paid to the possibilities of capacitance measurements for studying a-Si:H/c-Si heterojunctions. Capacitance versus voltage (*C-V*) or capacitance versus frequency and temperature (*C-ω-T*) and deep-level transient spectroscopy (DLTS) techniques at low temperatures were proposed in order to study defects at the a-Si:H/c-Si interface or the role of the inversion layer at the c-Si surface.[5–9]

In preceding works,[10,11] the temperature dependence of the capacitance of (p) a-Si:H/(n) c-Si solar cells in a wide temperature range, from 100 K up to 400 K, was presented. An overall frequency independent increase of capacitance with temperature was revealed. This strong capacitance increase is much larger than expected from the usual depletion approximation model and can be well reproduced by an explicit analytical calculation of the junction capacitance if one takes into account the existence of the strongly inverted layer at the c-Si surface that was earlier evidenced from other experimental techniques.[12,13]

In this paper, we recall the depletion approximation for calculating the capacitance of a (p) a-Si:H/(n) c-Si heterojunction and present the detailed procedure for the complete analytical calculation of the capacitance for the case of a (p) a-Si:H/(i) a-Si:H/(n) c-Si heterojunction. First, the case of a (p) a-Si:H/(n) c-Si heterojunction without (i) a-Si:H layer and with a semi-infinite (p) a-Si:H layer is described and compared to a simplified analytical calculation under the depletion approximation. Then, the introduction of the (i) a-Si:H layer is considered and its influence is discussed. At last, we introduce the finite thickness of the (p) a-Si:H layer and the front electrode in order to model the full transparent conductive oside (TCO)/(p) a-Si:H/(i) a-Si:H/(n) c-Si solar cell structure and discuss the influence of the TCO work function. Essential modifications of the calculating procedure are provided, and the influence of different parameters on the capacitance-temperature evolution is studied.

II. THEORETICAL DEVELOPMENT

A schematic view of the equilibrium band diagram of a (p) a-Si:H/(i) a-Si:H/(n) c-Si heterojunction is shown in Fig. 1. The total diffusion potential, $V_{d,}$ reads

$$qV_d = E_g^{c-Si} - \delta^{c-Si} + \Delta E_V - \delta^{a-Si:H}, \qquad (1)$$

where $E_g{}^{c\text{-}Si}$ is the c-Si band gap, $\delta^{a\text{-}Si:H}$ and $\delta^{c\text{-}Si}$ are the positions of the Fermi level referred to the majority carrier band in (p) a-Si:H and (n) c-Si, respectively, with $\delta^{c\text{-}Si} = k_BT\ln(N_C/N_d)$, k_B being the Boltzmann's constant, T being the temperature, N_C being the effective density of states (DOS) in the conduction band, and N_d being the donor density in c-Si. In this expression, ΔE_V is the band offset between the valence bands in (n) c-Si and (p) a-Si:H. It has to be stressed that Eq. (1) remains valid even if the band gap

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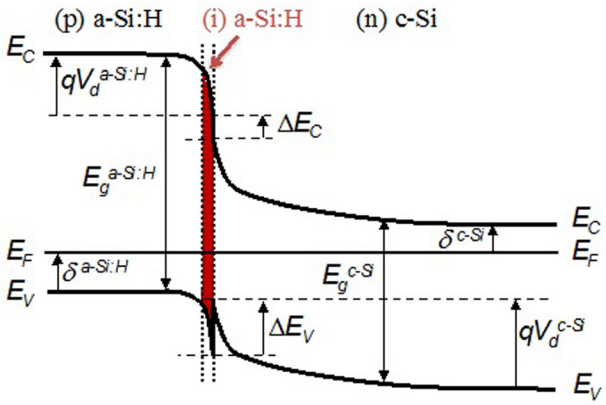


FIG. 1. Band diagram of the (p) a-Si:H/(n) c-Si heterojunction at equilibrium. The red area indicates the buffer layer that is used for passivation in high efficiency solar cells (for our experimental data, (i) a-Si:H was used).

of (i) a-Si:H is different from that of (p) a-Si:H, or if the (i) a-Si:H buffer is replaced by another material whatever the bandgap.

In this section, in order to draw the main features of the calculation, we neglect the existence of the "i" buffer layer, and we consider the (p) a-Si:H layer as semi-infinite. The (i) a-Si:H buffer layer and the finite thickness of the (p) a-Si:H layer will be implemented in the calculation, and their influence on the capacitance will be discussed in Sections III A and III B, respectively.

The two regions occupied by a-Si:H ($x<0$) and by c-Si ($x>0$) have to be treated separately, since the two semiconductors are very different in terms of defects determining the space charge density. We will first recall the traditional depletion layer approximation in c-Si[14] and show how to deal with a-Si:H, then we will provide the full analytical calculation.

A. Depletion approximation

Within the depletion approximation, the space charge density in c-Si can be approximated by a constant value $\rho(x)=qN_d^{c\text{-}Si}$, $N_d^{c\text{-}Si}$ being the donor doping density (supposed fully ionized), over a distance $w^{c\text{-}Si}$, while being equal to zero for $x>w^{c\text{-}Si}$. Then, the potential drop in c-Si can be written as

$$V_d^{c-Si}=\frac{qN_d^{c-Si}}{2\varepsilon}(w^{c-Si})^2+\frac{k_BT}{q}, \tag{2}$$

with q being the unit (positive) charge, and ε being the permittivity of c-Si. The total charge (all charges and capacitances in the following will be expressed by unit area) in c-Si is:

$$Q^{c-Si}=qN_d^{c-Si}w^{c-Si}. \tag{3}$$

In a-Si:H, the space charge density and the band bending are essentially related to the DOS at the Fermi level. We have shown that a very good description is obtained by assuming that the DOS, $N(E)^{a\text{-}Si:H}$, is equal to the DOS value at E_F in bulk a-Si:H.[13] This is because $N(E_F)^{a\text{-}Si:H}$ is significantly large such that the potential drop in (p) a-Si:H is much smaller than in c-Si, and the exact form of the DOS in a-Si:H (generally assumed to be the sum of exponential band tails and deep Gaussian distributions) has no significant influence. Considering exponential dependence of the potential in a-Si:H, one obtains a simple formulation of the total charge in a-Si:H

$$Q^{a-Si:H}=-\frac{\varepsilon}{L_D^{a-Si:H}}V_d^{a-Si:H}, \tag{4}$$

where the same permittivity ε as in c-Si is taken, $V_d^{a\text{-}Si:H}$ is the potential drop in a-Si:H, and $L_D^{a\text{-}Si:H}$ is the Debye length in a-Si:H, that is related to $N(E_F)^{a\text{-}Si:H}$ by

$$L_D^{a-Si:H}=\sqrt{\frac{\varepsilon}{q^2N(E_F)^{a-Si:H}}}. \tag{5}$$

We consider the overall charge neutrality

$$Q^{a-Si:H}+Q^{c-Si}+Q^{interface}=0, \tag{6}$$

where $Q^{interface}$ represents the charge of interface defects. However, we underline that, in a high efficiency solar cell, the passivation of the crystalline silicon surface by a-Si:H leads to interface defect densities that are in the 10^{10}–$10^{12}\,\mathrm{cm}^{-2}$ range.[15] This is low enough that no significant contribution of interface defects to the band bending nor in the device capacitance at zero bias in the dark can be found. Thus, rewriting the charge neutrality condition neglecting the interface charge and taking into account Eqs. (3) and (4), we obtain the following expression:

$$V_d^{a-Si:H}=\sqrt{V_1\left(V_d^{c-Si}-\frac{k_BT}{q}\right)}. \tag{7}$$

V_1 being the characteristic potential given by

$$V_1=\frac{2qN_d}{\varepsilon}\left(L_D^{a-Si:H}\right)^2. \tag{8}$$

Writing $V_d^{a\text{-}Si:H}$ as the difference between the total diffusion potential V_d and $V_d^{c\text{-}Si}$, Eq. (7) can be transformed into an equation that can be solved to deduce $V_d^{c\text{-}Si}$

$$V_d^{c-Si}=V_d-\frac{1}{2}\left[\sqrt{V_1\left(4V_d+V_1-\frac{4k_BT}{q}\right)}-V_1\right]. \tag{9}$$

Eq. (9) can be extended when a bias V_a is applied to the junction by replacing V_d by V_d-V_a. It can be used to study how the total potential drop is shared between a-Si:H and c-Si as a function of the various material parameters in both a-Si:H and c-Si and of the applied bias.

We are interested here in the quasistatic capacitance that can be measured at low frequencies. This is based on the estimation of the charge dQ that is extracted from one electrode with a change in terminal voltage dV_a

$$C=\frac{dQ}{dV_a}. \tag{10}$$

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Since the number of extracted electrons from one side equals the number of extracted holes from the other side, within the depletion approximation considered here, $dQ = dQ^{a\text{-}Si:H} = -dQ^{c\text{-}Si}$. Starting from

$$dV_a = -dV_d^{c-Si} - dV_d^{a-Si:H}, \tag{11}$$

and differentiating Eqs. (2)–(4), it is easy to show that

$$C = \frac{\varepsilon}{L_D^{a-Si:H} + w^{c-Si}}, \tag{12}$$

that explains that the equivalent total space charge width is the sum of the space charge width in c-Si and the Debye length in a-Si:H. Thus, obtaining $V_d{}^{c\text{-}Si}$ from Eq. (9) and then $w^{c\text{-}Si}$ from Eq. (2) allows us to calculate the quasistatic capacitance within the depletion approximation.

B. Full analytical calculation

In c-Si, we introduce the functions $u_e(x)$ and $u_h(x)$ to define the position of the electron and hole quasi Fermi levels

$$u_e(x) = \frac{E_F^e - E_i(x)}{k_B T}, \tag{13}$$

$$u_h(x) = \frac{E_F^h - E_i(x)}{k_B T}, \tag{14}$$

where $E_i(x)$ is the intrinsic level in c-Si as a function of distance x from the junction (where $x = 0$). Here, we assume that quasi Fermi levels E_F^h and E_F^e are independent of x in the space charge region with E_F^e corresponding to the bulk Fermi level. The splitting of the quasi Fermi levels is equal to qV_a, V_a being the voltage applied across the junction, and q being the (positive) unit charge. We can then write the electron and hole concentrations (n and p, respectively) in n-type c-Si as follows:

$$n(x) = n_i \exp u_e(x), \tag{15}$$

$$p(x) = n_i \exp(-u_e(x)) \exp \frac{qV_a}{k_B T}. \tag{16}$$

Eq. (16) is strictly valid only in the range where the quasi Fermi levels can be assumed flat; however, we can extend it to the whole c-Si to express the space charge density ρ

$$\rho(x) = q\left[n_i \exp(-u_e(x)) \exp \frac{qV_a}{k_B T} - n_i \exp u_e(x) + N_d^{c-Si}\right]. \tag{17}$$

Since we do not consider strong positive voltages and the concentration of holes becomes negligible as we move away from the junction, $u_e \gg qV_a/k_B T$ and we can express the doping density in terms of u_e far from the interface

$$N_d^{c-Si} \approx n_i \exp u_e(\infty). \tag{18}$$

The first term in the right hand side of Eq. (17) is usually neglected in the space charge layer under the depletion approximation. However, by introducing it into the calculations, one will be able to estimate whether its influence is negligible or not. Poisson's equation is then written in terms of the variable $u_e(x)$

$$\frac{d^2 u_e}{dx^2} + \frac{q^2 n_i}{\varepsilon k_B T}\left[\exp\left(-u_e(x) + \frac{qV_a}{k_B T}\right) - \exp u_e(x) + \exp u_e(\infty)\right] = 0. \tag{19}$$

After multiplication of both sides of Eq. (19) by the term $2du_e/dx$, and further integration, we obtain the following expression:

$$L_D^{c-Si} \frac{du_e}{dx} = \sqrt{f(u_e(x), V_a)}, \tag{20}$$

with

$$f(u_e(x), V_a) = \exp u_e(x) + \exp\left(-u_e(x) + \frac{qV_a}{k_B T}\right) - \exp u_e(\infty) - \exp\left(-u_e(\infty) + \frac{qV_a}{k_B T}\right) + \exp u_e(\infty) \cdot \left(u_e(\infty) - u_e(x)\right), \tag{21}$$

and L_D^{c-Si} being the intrinsic Debye length in (n) c-Si

$$L_D^{c-Si} = \sqrt{\frac{\varepsilon k_B T}{2q^2 n_i}}. \tag{22}$$

The positive sign has been chosen in Eq. (20), since the electric field is here negative in this p-n heterojunction. The total charge in c-Si can then be expressed as

$$Q^{c-Si} = \frac{\varepsilon k_B T}{q} \frac{1}{L_D^{c-Si}} \sqrt{f\left(u_e(0), V_a\right)}. \tag{23}$$

The total charge in a-Si:H given by Eq. (4) can also be expressed as a function of $u_e(0)$, since the potential drop in a-Si:H can be written as

$$qV_d^{a-Si:H} = qV_d - qV_a - k_B T(u_e(\infty) - u_e(0)), \tag{24}$$

with V_d the total diffusion potential at equilibrium as given by Eq. (1). Thus, rewriting the charge neutrality condition neglecting the interface charge and taking into account Eqs. (1), (4), (23), and (24), we obtain

$$\frac{E_G^{c-Si} - \delta^{c-Si} + \Delta E_V - \delta^{a-Si:H} - qV_a - k_B T\left(u_e(\infty) - u_e(0)\right)}{L_D^{a-Si:H}} = \frac{k_B T}{L_D^{c-Si}} \sqrt{f\left(u_e(0), V_a\right)}, \tag{25}$$

with only one unknown variable, namely, $u_e(0)$. One can note that the right hand side that reflects the charge in c-Si is a decreasing function of $u_e(0)$ for $u_e(0) < u_e(\infty)$ (that holds in our case of a p-n junction), while the left hand side is an increasing function of $u_e(0)$. Therefore, a single-valued analytical solution can be obtained from which one can calculate the charges in a-Si:H and c-Si and study their dependence as

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a function of a-Si:H parameters, total diffusion potential, and applied voltage. Without going into all details, it is worth emphasizing some features that can be deduced at equilibrium from Eq. (25) due to the monotonous variations of both sides with $u_e(0)$. If $u_e(0) < -u_e(\infty)$, a strong inversion layer builds at the c-Si surface where the contribution of holes will then dominate in the space charge density. An increase in $\Delta E_V - \delta^{a\text{-}Si:H}$ will lead to a lower value of $u_e(0)$ corresponding to stronger band bending in c-Si which can thus promote the formation of such a strong hole inversion layer. For the same reason, a decrease of the Debye length in a-Si:H (i.e., an increase of the DOS at the Fermi level in a-Si:H) will also lead to a lower value of $u_e(0)$ meaning that an increase of the DOS in a-Si:H will increase the band bending in c-Si while decreasing the band bending in a-Si:H, which also can promote the formation of a strong hole inversion layer at the c-Si surface.

The capacitance can then be obtained again from Eq. (10). Since there are almost no electrons on the (p) a-Si:H side, the charge Q in Eq. (10) is the charge of extracted electrons Q_e from the c-Si, given by

$$Q_e = \int_0^\infty q(N_D^{c-Si} - n(x))dx, \tag{26}$$

which can be rewritten using u_e as the variable

$$Q_e = qn_i L_D^{c-Si} I, \tag{27}$$

with

$$I = \int_{u_e(0)}^{u_e(\infty)} \frac{\exp u_e(\infty) - \exp u_e}{\sqrt{f(u_e, V_a)}} du_e. \tag{28}$$

The capacitance is thus given by

$$C = qn_i L_D^{c-Si} \frac{dI}{dV_a}. \tag{29}$$

With the help of a MATLAB software, the capacitance is calculated according to Eq. (29) as a function of temperature and applied voltage for different values of the valence band offset, density of states in a-Si:H, and position of the equilibrium Fermi level within the bandgap (related to doping) in c-Si and a-Si:H. It is worth emphasizing that based on the equations given above one can also calculate the capacitance without taking into account the holes and consequently neglecting the strong inversion layer in c-Si if any. If one neglects the holes' contribution to the charge density in Eq. (17), the function f is then reduced to f^* that is independent of V_a

$$f^*(u_e(x)) = \exp u_e(x) - \exp u_e(\infty) + \exp u_e(\infty)(u_e(\infty) - u_e(x)), \tag{30}$$

and the capacitance is obtained from Eq. (29) by following the same procedure as given above and substituting f by f^*.

The inversion layer issue was addressed for the first time by Gummel and Scharfetter while calculating the capacitance for crystalline p^+–n homojunctions.[16] These authors showed through the example of a p^+–n junction that the depletion approximation was not valid if one side of the junction is much more heavily doped than the other, namely, for the determination of the intercept voltage in a plot of C^{-2} vs applied voltage. It was suggested by the authors that there was the spill-over charge influencing the capacitance value which was proved by adding the essential term of the holes contribution to the charge in the n-side of the junction. This early work has been followed by contributions from other authors.[17,18] Also, calculations of the capacitance of silicon heterojunctions have been presented by Rubinelli.[19,20] However, the temperature dependence of the capacitance and the link to the minority carriers inversion change have not been studied so far in the literature.

III. RESULTS AND DISCUSSION

A. Depletion approximation

In this section, we present the results of capacitance calculated as described in Section II A using, namely, Eq. (12). Influence of different parameters on the obtained capacitance-temperature dependencies is discussed.

Since the capacitance of a heterojunction can be considered as two capacitances put in series, in the case of a (p) a-Si:H/(n) c-Si heterojunction, it is interesting to estimate the contribution of each layer to the total capacitance signal. In Figure 2, one can see the influence of the DOS at the Fermi level in a-Si:H, $N(E_F)$, on the temperature evolution of the capacitance of the (n) c-Si layer and that of the heterojunction. As one can see with the increase of $N(E_F)$, the potential drop in c-Si increases according to Eq. (9) that results in the decrease of capacitance of the c-Si layer. On the other hand, the a-Si:H layer's capacitance grows with the increase of $N(E_F)$. These two tendencies balance each other giving a weak dependency of the heterojunction capacitance on the DOS at the Fermi level in a-Si:H that becomes negligible from $N(E_F) = 10^{17}\,\mathrm{eV}^{-1}\,\mathrm{cm}^{-3}$. Thus, the defect density in the p-type amorphous layer brings little influence to the capacitance.

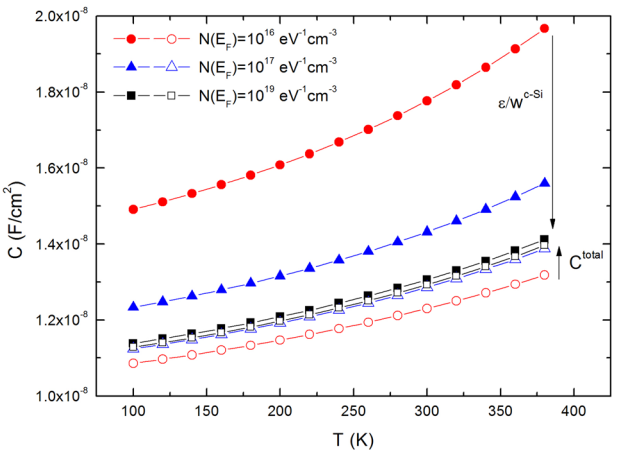


FIG. 2. Temperature dependencies of the (n) c-Si capacitance (full symbols) and of the capacitance of (p) a-Si:H/(n) c-Si heterojunction (open symbols) for different values of the DOS at the Fermi level in (p) a-Si:H.

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TABLE I. Input values of physical parameters fixed for all full analytical calculations presented in this work. The temperature dependence of the bandgap and effective densities of states in the conduction and valence band in crystalline silicon have been taken from Refs. 23 and 24.

Parameter	Value
$N_d^{c\text{-}Si}$	$1.5 \times 10^{15}\,\mathrm{cm}^{-3}$
$\delta^{a\text{-}Si:H}$	0.45 eV
$N(E_F)$	$1 \times 10^{19}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$
E_g^{c-Si}	$1.1692 - \frac{4.9 \times 10^{-4} T^2}{T + 655}$
$E_g^{a-Si:H}$	$1.8\text{–}2.25 \times 10^{-4} T$
N_C^{c-Si}	$2.89 \times 10^{19} \left(\frac{T}{300}\right)^{1.58}$
N_V^{c-Si}	$3.0 \times 10^{19} \left(\frac{T}{300}\right)^{1.85}$

Another important question is how the temperature evolution of the capacitance changes when temperature dependencies of physical parameters describing two considered materials are introduced. Since the potential drop in (n) c-Si is defined through the total diffusion potential (Eq. (1)), temperature dependencies of all involved parameters may influence the capacitance. The temperature dependence of c-Si parameters is summarized in Table I.

That $\delta^{c\text{-}Si}$ is obtained assuming full ionization of the donor atoms in the explored temperature range

$$\delta^{c-Si} = k_B T \ln\left(\frac{N_C}{N_d^{c-Si}}\right). \tag{31}$$

The only temperature dependence that is not well identified in Eq. (25) is that of ΔE_V-$\delta^{a\text{-}Si:H}$. In first approximation, we introduced a linear dependence

$$\Delta E_V - \delta^{a-Si:H} = E_0 - \alpha T, \tag{32}$$

where E_0 is the value at 0 K. We first set $\alpha = 0$ and varied E_0 in order to determine the value that best matches with the experimental C-T data at low temperature (around -0.05 eV). However, as can be seen in Fig. 3, the temperature dependence is much weaker than observed in the experimental data. Then, physically acceptable values of the temperature coefficient α were introduced.[10,21,22] The temperature dependence of the calculated capacitance can be increased when increasing α. However, up to very high values of α, the C-T dependence calculated from the depletion approximation remains too weak. This led us to the conclusion that the depletion theory capacitance fails to reproduce the observed experimental temperature dependence and one has to consider the full analytical calculation including the contribution of holes in (n) c-Si.

B. Full analytical calculation

As detailed in Section II B, the full analytical calculation allows one to take into consideration minor carriers in the space charge density, namely, holes for the case of (n) c-Si. Therefore, the first issue to address is to estimate the contribution of holes in (n) c-Si to the capacitance of (p) a-Si:H/(n) c-Si heterojunction.

To this purpose, we calculate the capacitance from Eq. (29) using the function f (Eq. (21) and f^* (Eq. (30)) for the two cases, with and without holes, respectively. The input values of the main parameters are listed in Table I. They remain unchanged for all calculations unless otherwise stated.

In Figure 4, C-T curves calculated from the full analytical approach at $\Delta E_V = 0.4$ eV are compared with the one obtained from the depletion approximation. For this value of the valence band offset, there is a significant influence of the holes in the (n) c-Si layer already at low temperatures that results in promoting the temperature evolution of the capacitance. On the other hand, the calculation without considering holes closely resembles the curve obtained with the depletion approximation, allowing us to conclude that taking holes into account has a major impact on the capacitance for certain values of the valence band offset.

Indeed, the contribution of the holes when taken into account in the calculations depends on the potential drop in c-Si that can be changed by changing the band offset while

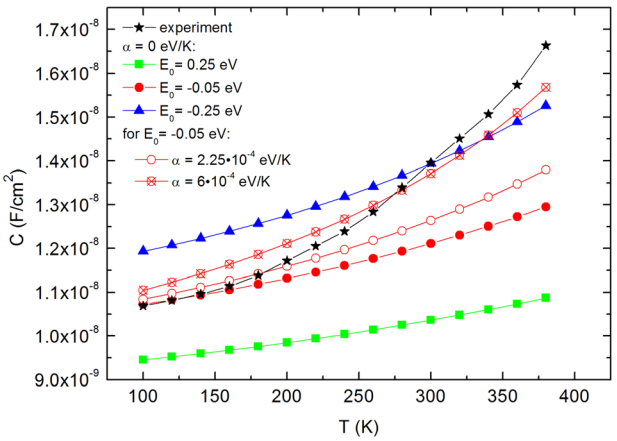


FIG. 3. Temperature dependent capacitance curves calculated within the depletion approximation compared to experimental data obtained on a high efficiency silicon heterojunction solar cell at zero bias (★). Full symbols correspond to $\alpha = 0$ and various values of E_0. Open symbols correspond to $E_0 = -0.05$ eV and two values of α.

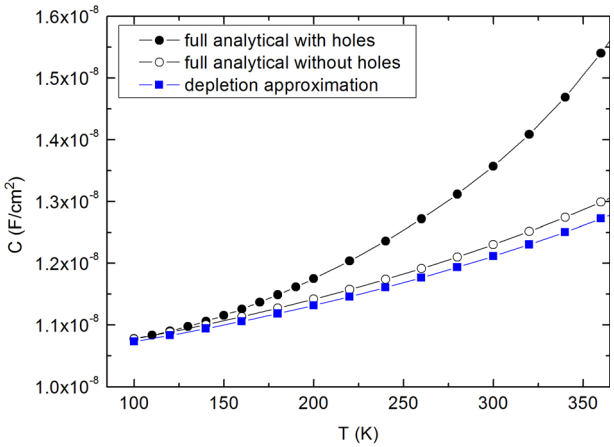


FIG. 4. Comparison of the capacitance-temperature dependencies at $\Delta E_V = 0.4$ eV calculated from the depletion approximation and full analytical calculation (full symbols—holes are taken into account in the charge density in (n) c-Si, open symbols—holes are neglected).

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keeping all other parameters constant, as seen from Eq. (1). For instance, the effect on the capacitance for three different values of ΔE_V can be seen in Fig. 5(a). For a low valence band offset, $\Delta E_V = 0.1$ eV, the contribution of holes is negligible in the whole temperature range because no strong inversion layer exists whatever the temperature. On the contrary, for $\Delta E_V = 0.5$ eV, we obtained two very different capacitance curves in the whole temperature range when comparing calculations that consider or ignore the presence of the holes. The case of $\Delta E_V = 0.3$ eV is intermediate: the two capacitance curves are identical below $T \approx 270$ K, while a stronger increase of the capacitance is observed at higher temperatures when holes are taken into account.

Now we show the parallel between the capacitance-temperature curves and the charge in (n) c-Si that emphasizes the importance of taking into account the holes' contribution to the space charge density.

The total space charge in c-Si can be expressed as

$$Q^{c-Si} = Q^{h,c-Si} + Q^{depl,c-Si}, \tag{33}$$

where $Q^{h,c\text{-}Si}$ and $Q^{depl,c\text{-}Si}$ are the charges due to holes and the depletion charge, given, respectively, by

$$Q^{h,c-Si} = q\int_0^\infty p(x)dx, \tag{34}$$

$$Q^{depl,c-Si} = q\int_0^\infty [N_d - n(x)]dx. \tag{35}$$

Note that the depletion charge is identical to that of the extracted electron charge given by Eq. (26). The c-Si wafer has a given thickness $d^{c\text{-}Si}$ (of the order of 150 μm) that is much larger than the thickness of the space charge layer, and the back contact can be considered as having negligible impact on the measured capacitance so we will neglect it here and consider the c-Si as semi-infinite. As one can see there is a strong correlation between *C-T* curves (Fig. 5(a)), and the comparison of the charges $Q^{h,c\text{-}Si}$ and $Q^{depl,c\text{-}Si}$ defined by Eqs. (34) and (35) and shown in Fig. 5(b). Indeed, for $\Delta E_V = 0.5$ eV, $Q^{h,c\text{-}Si}$ is larger than $Q^{depl,c\text{-}Si}$ in the whole temperature range confirming the conclusion of the existence of the strong inversion. Therefore, the two capacitances calculated with or without including the holes in the space charge density calculation are different. On the opposite, for $\Delta E_V = 0.1$ eV, $Q^{h,c\text{-}Si}$ is negligible in comparison with $Q^{depl,c\text{-}Si}$ in the whole temperature range, and the two capacitances calculated with or without including the holes are identical. Finally, for the case $\Delta E_V = 0.3$ eV, $Q^{h,c\text{-}Si}$ is much smaller than $Q^{depl,c\text{-}Si}$ below 270 K, where the two capacitances calculated with or without including the holes are identical.

So far we showed that, in the presence of strong inversion in (n) c-Si, the capacitance evolution with temperature is strongly enhanced. In order to provide a physical explanation of this phenomenon, we recall that the junction capacitance in a p-n junction can be written as[25]

$$C = \frac{\varepsilon}{\langle x^e \rangle - \langle x^h \rangle}, \tag{36}$$

where $\langle x^e \rangle - \langle x^h \rangle$ is the separation between the first momentum of charge variation due to electrons from the n-side and that due to holes from the p-side following a small change of applied bias. Charge variations due to electrons occur at the edge of the space charge region in c-Si, $w_{c\text{-}Si}$, so that $\langle x^e \rangle \approx w_{c\text{-}Si}$. When no strong inversion exists at the c-Si surface, the charge variation due to holes occurs in a-Si:H at a mean distance $L_D^{a-Si:H}$ from the junction, so that $\langle x^h \rangle \approx L_D^{a-Si:H}$. This leads to the expression (12) for the capacitance. Since $L_D^{a-Si:H}$ is generally much smaller than $w_{c\text{-}Si}$ and weakly temperature dependent, the temperature dependence of the capacitance then mainly comes from the temperature dependence of $w_{c\text{-}Si}$. This in turn is related to the temperature dependence of the potential drop in c-Si, $V_d^{c\text{-}Si}$, that can be obtained from the classical depletion approximation described at the beginning of Section II

$$qV_d^{c-Si,depl.appox}(T) = E_g^{c-Si} + \left[\Delta E_V - \delta^{a-Si:H} - qV_d^{a-Si:H}\right](T) - k_B T \ln\frac{N_C(T)}{N_d}. \tag{37}$$

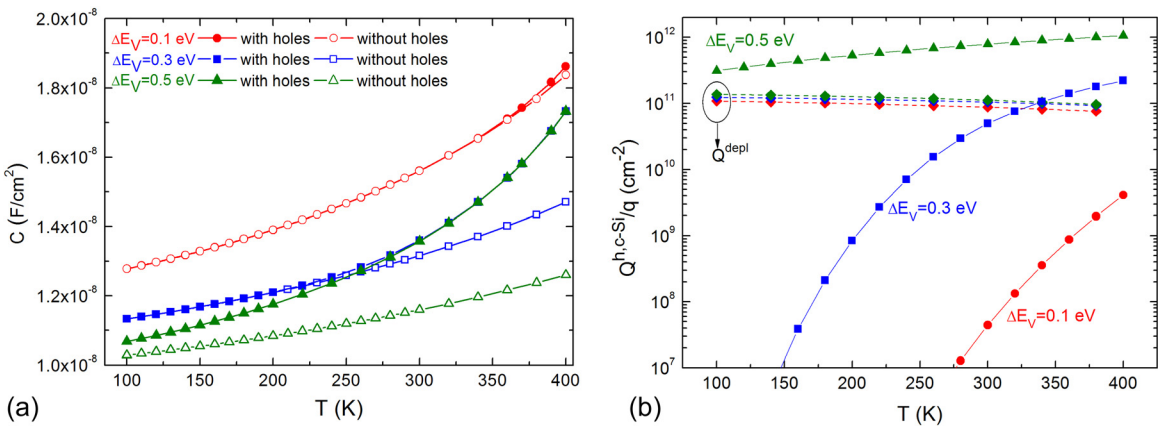


FIG. 5. (a) Temperature dependence of the capacitance from the full analytical calculation for three values of the valence band offset. The full symbols show the result of the full calculation that takes into account the holes in the space charge density, while the open symbols correspond to the calculation where the contribution of holes has been suppressed. (b) Corresponding calculated temperature dependence of the charge due to holes in (n) c-Si ($Q^{h,c\text{-}Si}$) for the three values of valence band offset. Also shown is the depletion charge that is much less sensitive to ΔE_V.

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The capacitance then varies with temperature like $1/\sqrt{V_d^{c-Si,depl.approx}(T)}$.

However, if a strong inversion layer exists at the c-Si surface, we can introduce the width of the strong inversion layer, x_{inv}, the width of the whole space charge layer still being denoted $w_{c\text{-}Si}$, as depicted in Fig. 6. In that case, we have $\langle x^e \rangle \approx w_{c\text{-}Si}$ while $\langle x^h \rangle \approx x_{inv}$. The interval $[x_{inv}, w_{c\text{-}Si}]$ is the region where the depletion approximation can be used. The potential drop in this region, named $V_d^{c\text{-}Si,inv.limited}$, is given by[10]

$$qV_d^{c-Si,inv.limitted}(T) = E_g^{c-Si}(T) - 2k_BT\ln\frac{\sqrt{N_c(T)N_V(T)}}{N_d}, \tag{38}$$

and this potential drop is related to the width of the depleted zone by

$$qV_d^{c-Si,inv.limited} = \frac{qN_d^{c-Si}}{2\varepsilon}\left(w^{c-Si} - x_{inv}\right)^2 + \frac{k_BT}{q}. \tag{39}$$

The capacitance variation with temperature is then close to $1/\sqrt{V_d^{c-Si,inv.limited}(T)}$. If we compare the expressions of $V_d^{c-Si,inv.limited}$ with that of $V_d^{c-Si,depl.approx}$, we can see that the main difference comes from the factor of 2 in the last term, since the temperature dependence of the central term $(\Delta E_V - \delta^{a\text{-}Si:H} - V_d^{a\text{-}Si:H})$ in Eq. (37) is weak compared to that of the two other ones. This enhances the temperature dependence of $V_d^{c-Si,inv.limited}$ compared to that of $V_d^{c-Si,depl.approx}$ and results in the stronger increase of capacitance with temperature in presence of a strong inversion layer.

In order to confirm that $V_d^{c-Si,inv.limited}$ indeed determines the temperature dependence of the capacitance under strong inversion conditions, we calculate the apparent diffusion voltage, V_d^{app}, obtained from capacitance data shown in Figure 4 according to[10]

$$V_d^{app}(T) = \frac{qN_d\varepsilon}{2}\left(\frac{1}{C}\right)^2. \tag{40}$$

In Figure 7, one can see that $V_d^{c-Si,inv.limited}$ is very close to V_d^{app} calculated from the full analytical approach with holes taken into account. V_d^{app} obtained from capacitance data calculated without holes follows V_d^{c-Si} calculated from the classical depletion approximation presented as well.

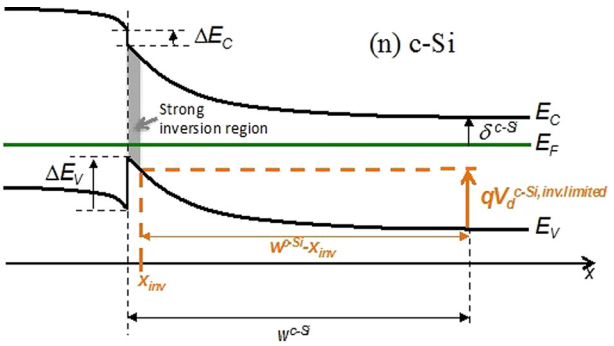


FIG. 6. Equilibrium band diagram at the (p) a-Si:H/(n) c-Si heterojunction with strong inversion region existing at the c-Si surface, showing the limit of the strong inversion region and the potential drop in the depleted region that is limited by the strong inversion region.

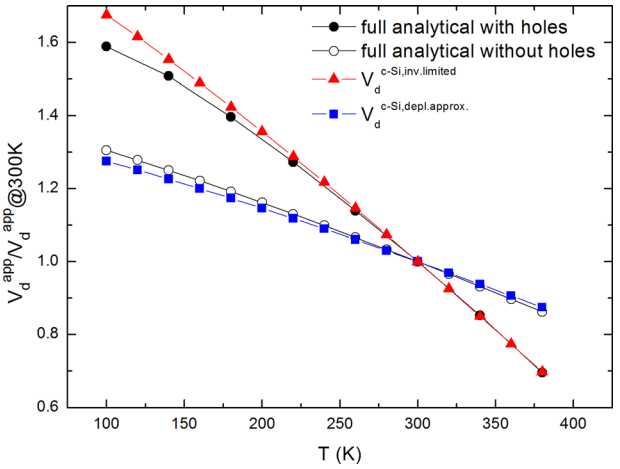


FIG. 7. Temperature dependence of V_d^{app} (normalized to its value at 300 K) calculated from capacitance data of Figure 4 ($\Delta E_V = 0.4$ eV). Also shown is $V_d^{c-Si,inv.limited}$ calculated from Eq. (38) (▲).

The slight difference at low T between $V_d^{c-Si,inv.limited}$ and V_d^{app} calculated including the contribution of holes is the result of a weakening or disappearance of the strong inversion at this temperature range for $\Delta E_V = 0.4$ eV.

C. Influence of the finite thickness of the (p) a-Si:H layer and of the (i) a-Si:H buffer layer

So far, we have always considered the (p) a-Si:H layer as semi-infinite. This is a reasonable assumption as a starting point to illustrate the temperature dependence of the capacitance, since the density of states at the Fermi level in (p) a-Si:H is large, thus providing strong shielding of the potential in a-Si:H. However, in actual heterojunction solar cells, the thickness of the (p) a-Si:H layer is also very small and can possibly become comparable to the Debye length. In that case, the finite thickness of the (p) a-Si:H layer and the charge developing at the electrode contacting the (p) a-Si:H have to be introduced in the calculation. In addition, a thin (i) a-Si:H buffer layer is introduced at the a-Si:H/c-Si interface for passivation purposes. In order to study how the finite thickness of (p) a-Si:H and the thin (i) a-Si:H buffer layer affect the junction capacitance, we introduced them in our analytical calculation. Details are given in the Appendix. It turns out that Eq. (25) that is used to determine the band bending in the structure has to be replaced by

$$\frac{qV_d - qV_a - k_BT\left(u_e(\infty) - u_e(0)\right)}{L_D^{a-Si:H}}\theta_1 - \frac{\Delta E_F}{L_D^{a-Si:H}}\theta_2 + \frac{\Delta WF}{L_D^{a-Si:H}}\theta_3 = \frac{k_BT}{L_D^{c-Si}}\sqrt{f\left(u_e(0), V_a\right)}, \tag{41}$$

where θ_1, θ_2, and θ_3 are correction terms that are given by

$$\theta_1 = \frac{\cosh\left(\frac{d_i}{L_i}\right) + \frac{L_D^{a-Si:H}}{L_i}\sinh\left(\frac{d_i}{L_i}\right)\tanh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right)}{\tanh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right)\cosh\left(\frac{d_i}{L_i}\right) + \frac{L_i}{L_D^{a-Si:H}}\sinh\left(\frac{d_i}{L_i}\right)}, \tag{42}$$

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$$\theta_2 = \frac{\cosh\left(\frac{d_i}{L_i}\right) + \frac{L_D^{a-Si:H}}{L_i}\sinh\left(\frac{d_i}{L_i}\right)\tanh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right) - 1}{\tanh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right)\cosh\left(\frac{d_i}{L_i}\right) + \frac{L_i}{L_D^{a-Si:H}}\sinh\left(\frac{d_i}{L_i}\right)}, \tag{43}$$

$$\theta_3 = \frac{1}{\sinh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right)\cosh\left(\frac{d_i}{L_i}\right) + \frac{L_i}{L_D^{a-Si:H}}\sinh\left(\frac{d_i}{L_i}\right)\cosh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right)}. \tag{44}$$

ΔE_F is the difference (positive) between the equilibrium Fermi level in (i) a-Si:H and in (p) a-Si:H, and $\Delta WF = \Phi^{a\text{-}Si:H} - \Phi^M$ is the difference in work function between (p) a-Si:H and the metal electrode (in a-Si:H/c-Si solar cells the contacting electrode at the (p) a-Si:H side often consists of a TCO layer, however our calculations apply whatever the nature of the contacting electrode, and we designate the contacting electrode as the "metal" electrode in the following). One can observe that Eq. (41) simplifies into Eq. (25) if the (i) a-Si:H layer has exactly the same properties as the (p) a-Si:H layer, i.e., if $L_i = L_D^{a-Si:H}$ and $\Delta E_F = 0$ and if the thickness of the (p) a-Si:H layer is much larger than the Debye length. We also note that θ_1, θ_2, and θ_3 are all positive.

In order to separate the effects, we first study the case where the (i) a-Si:H buffer layer is introduced while keeping an infinite (p) a-Si:H layer, then we consider the case of a finite (p) a-Si:H layer without (i) buffer layer. Finally, we consider the case where both finite (p) a-Si:H thickness and (i) buffer layer are introduced.

1. Introduction of the (i) a-Si:H buffer layer with infinite (p) a-Si:H

In this case, only the two first terms in Eq. (41) are to be considered since $\theta_3 = 0$. We then also note that $0 < \theta_1 < 1$, since the DOS in (i) a-Si:H should be lower than that in (p) a-Si:H. Therefore, due to the monotonous variation of both sides of Eq. (25) with $u_e(0)$, the introduction of an (i) a-Si:H buffer layer will lead to an increased value of $u_e(0)$. As a consequence, if a strong hole inversion layer does exist at the c-Si surface without (i) a-Si:H buffer layer, the introduction of an (i) a-Si:H buffer layer leads to a weaker strong inversion layer or to the suppression of it.

In order to reveal the influence of the (i) a-Si:H layer on the capacitance-temperature dependency, we varied the value of the density of states in the (i) a-Si:H layer considered constant throughout the bandgap, N_i, starting from $10^{16}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$—a typical value for thick undoped amorphous silicon, up to the DOS value in (p) a-Si:H (nominal value taken at $10^{19}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$), and $\Delta E_F = 0.65\,\mathrm{eV}$—also a typical value for the change in Fermi level position between (p) and (i) a-Si:H, and we also varied the thickness of the (i) a-Si:H layer. For the sake of clarity, the comparison is presented using the term of apparent diffusion voltage obtained from *C-T* data according to Eq. (40). First, we would like to address the influence of N_i at 10 nm thickness. For $N_i = 10^{16}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$, no difference could be seen between the data calculated without (i) buffer layer and that calculated with $d_i = 10\,\mathrm{nm}$ (data not shown). If one increases N_i to $10^{17}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$, a slight difference can be observed for $\Delta E_V = 0.1\,\mathrm{eV}$ in the whole temperature range but with no significant change in the slope, as it can be seen in Figure 8(a). Further increase of N_i results in an enhanced

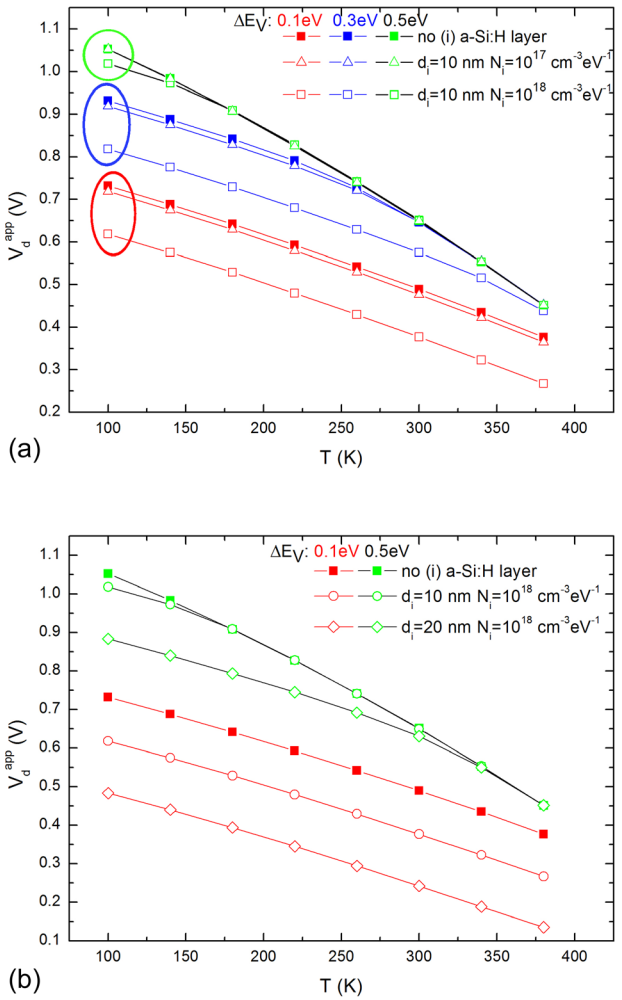


FIG. 8. (a) Temperature dependence of V_d^{app} obtained from capacitance data calculated with and without (i) a-Si:H buffer layer (full symbols for no (i) a-Si:H layer and open symbols for 10 nm) for $\Delta E_V = 0.1\,\mathrm{eV}$, 0.3 eV, and 0.5 eV. (b) Influence of the various (i) a-Si:H layer thickness (no (i) a-Si:H layer, $d_i = 10$ and 20 nm) on the temperature dependence of V_d^{app}.

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increase of capacitance therefore a decrease of V_d^{app}, again with no significant change in the slope. This reflects a decrease of the band bending in c-Si. Indeed, increasing N_i corresponds to decreasing L_i which leads to an increase of θ_1 and θ_2. This in turn leads to a larger value of $u_e(0)$ from Eq. (41). We have seen above that in the absence of the (i) a-Si:H buffer no strong inversion layer exists at the c-Si surface for $\Delta E_V = 0.1$ eV. Thus, introducing the (i) layer reduces the band bending and width of the depletion layer in c-Si, thus reducing V_d^{app} but the temperature dependence is not strongly affected because the c-Si remains in a depletion regime. For $\Delta E_V = 0.3$ eV, we can observe that increasing N_i to $10^{18}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$ leads to a decrease of V_d^{app} with a reduced slope above 250 K compared to the case without (i) buffer layer. This reflects the disappearance of the strong inversion layer above 250 K. For $\Delta E_V = 0.5$ eV, we have seen above that the strong inversion layer exists almost in the whole temperature range without (i) buffer layer. Introducing the (i) buffer layer only produces an effect for $N_i = 10^{18}\,\mathrm{cm}^{-3}\,\mathrm{eV}^{-1}$ at low temperature where the strong inversion layer then tends to disappear as reflected by the decrease of V_d^{app} together with a weaker slope.

The influence of the (i) buffer layer's thickness on the apparent diffusion voltage is shown in Fig. 8(b) for the two extreme values of ΔE_V. The increase of the (i) thickness from 10 nm to 20 nm results in a decrease of θ_1 and an increase of θ_2, leading to an increase of $u_e(0)$. This results in a weaker band bending in c-Si. For $\Delta E_V = 0.1$ eV, this is reflected by the decrease of V_d^{app} in the whole temperature range. For $\Delta E_V = 0.5$ eV, this decrease of band bending implies that the strong inversion layer now appears only at higher temperature (>350 K) as reflected in the change of slope.

Based on these results, we can conclude that the introduction of an (i) a-Si:H buffer layer reduces the band bending in c-Si, which can weaken or even suppress the strong hole inversion layer at the c-Si surface if this exists in the absence of buffer layer. As long as strong inversion exists the average position of the charge variations due to refilling of holes from the p-side and of electrons from the n-side is almost unchanged, and the capacitance is almost unchanged. The strong inversion layer tends to disappear first at low temperature, which is then reflected in a smaller apparent diffusion voltage extracted from the junction capacitance, together with a weaker temperature dependence. For solar cell applications, the (i) a-Si:H layer is very thin, typically below 5 nm. The above calculations show that the influence on the capacitance and on its temperature dependence is then very weak and might be only seen at low temperature if strong inversion conditions prevail at room temperature ($\Delta E_V > 0.3$ eV).

2. Introduction of the finite thickness of the (p) a-Si:H layer without (i) a-Si:H buffer layer

In this case, $\theta_2 = 0$ and only the first and third terms in Eq. (41) have to be considered. We studied how the capacitance-temperature curves are modified by changing the (p) a-Si:H layer thickness and the difference in work functions, ΔWF.

First, we fixed the work function of the material of the electrode, $q\Phi^M$, at 4.9 eV, thus creating a Schottky contact at the front interface of the cell due to a negative value of ΔWF since the work function of (p) a-Si:H is set here to 5.18 eV (at 300 K). This leads to an increase of $u_e(0)$ as compared to the case of infinite (p) a-Si:H thickness. Indeed, when the thickness of the (p) a-Si:H layer becomes comparable or smaller than the Debye length, the effect of the band bending at the metal/(p) a-Si:H interface can extend to the (p) a-Si:H/c-Si interface. For the nominal DOS in (p) a-Si:H taken in our calculations, the Debye length is of 7.9 nm. Therefore, reducing the thickness of (p) a-Si:H to 25 nm has almost no effect, while some significant change can be observed for 10 nm. For $\Delta E_V = 0.1$ eV, where no strong inversion exists at the c-Si surface for infinite (p) a-Si:H, the further reduction of the band bending due to the decrease of the (p) a-Si:H thickness results in a smaller apparent diffusion voltage as can be seen in Figure 9. This corresponds to a reduced width of the depletion region in c-Si and consequently to an increased junction capacitance. For $\Delta E_V = 0.3$ eV, where

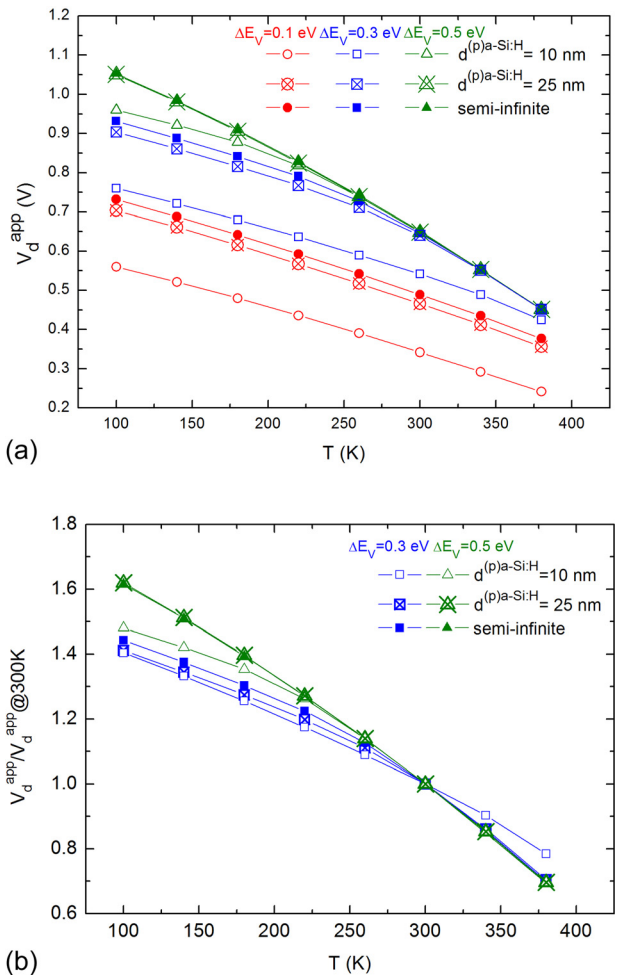


FIG. 9. (a) Comparison of temperature dependencies of V_d^{app} obtained from *C-T* data for different thicknesses of the (p) a-Si:H layer ($d^{(p)a\text{-}Si:H} = 10$ nm, 25 nm, and semi-infinite) for $\Delta E_V = 0.1$ eV, 0.3 eV, and 0.5 eV. The work function of the electrode is set at $q\Phi^M = 4.9$ eV. (b) Temperature dependence of V_d^{app} normalized to the value at 300 K for $\Delta E_V = 0.3$ eV and 0.5 eV.

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strong inversion conditions at the c-Si surface exist above 250 K for infinite (p) a-Si:H, decreasing the (p) layer thickness to 10 nm and thus decreasing the band bending can suppress this strong inversion, as inferred from the weaker slope of the apparent diffusion voltage. Finally, for $\Delta E_V = 0.5$ eV, all the curves of normalized $V_d^{app}(T)$ coincide except at low temperatures (<250 K) for $d = 10$ nm. This again can be explained by the fact that the strong inversion which exists in the whole temperature range for infinite (p) layer thickness is reduced by the thin (p) a-Si:H layer and its band bending at the front contact.

In order to further emphasize how the contact electrode on the (p) a-Si:H layer can affect the capacitance curves, we have varied the work function of the electrode metal while keeping the (p) a-Si:H layer at $d_{a\text{-}Si:H} = 10$ nm. This is illustrated in Fig. 10 for three values of Φ^M corresponding to three values of ΔWF at 300 K, and for two values of ΔE_V. For $\Delta E_V = 0.5$ eV and for positive values of ΔWF, the capacitance-temperature curve is the same as for an infinite (p) a-Si:H layer. This is because a positive value of ΔWF can only reinforce the strong inversion layer at the c-Si surface. The capacitance-temperature curve is thus fully determined by the strong inversion layer as explained in Section III B, and it does not depend on ΔWF. For small negative values of ΔWF, only a very slight change can be observed below 150 K. For larger negative values of ΔWF, the deviation from the infinite (p) a-Si:H case is more pronounced, and the temperature range where this deviation is visible is extended. Thus, for $q\Phi^M = 4.9$ eV, a flattening of the temperature dependence of the capacitance can be seen up to 225 K because the strong inversion layer has disappeared in this temperature region, while above 225 K the strong inversion layer still persists. The effect of the metal/(p) a-Si:H contact is more pronounced for $\Delta E_V = 0.3$ eV because there was already a transition for infinite (p) a-Si:H between a high temperature regime ($T > 250$ K) where strong inversion determined the temperature behavior and a low temperature regime ($T < 250$ K) where strong inversion did not exist at the c-Si surface. Introducing a Schottky barrier at the metal/(p) a-Si:H contact can thus extend the temperature range where no strong inversion exists at the c-Si surface. This can be seen in Fig. 10 for $q\Phi^M = 5$ eV where the flattening of the temperature dependence of the capacitance is visible almost up to 380 K. If we further decrease $q\Phi^M$ to 4.9 eV, the c-Si surface is never under strong inversion in the explored temperature range. Moreover, the band bending due to the Schottky barrier at the metal/(p) a-Si:H contact extending to the a-Si:H/c-Si interface causes a decrease of the potential drop in c-Si, and consequently a decrease of the width of the depletion region. This in turn leads to an overall increase of the capacitance in the whole temperature range. On the contrary, for positive values of $\Delta WF(q\Phi^M = 5.3$ eV), the band bending at the metal/(p) a-Si:H contact is of opposite sign. This favours the creation of a strong inversion layer at the c-Si surface compared to the infinite a-Si:H case. This is revealed in Fig. 10 by the fact that the capacitance curve is closer to that corresponding to $\Delta E_V = 0.5$ eV than for an infinite (p) a-Si:H layer.

So far we observed that significant changes to the capacitance behavior compared to the case of an infinite (p) a-Si:H layer appeared for a thickness of 10 nm. However, the important factor is not the thickness of the (p) a-Si:H layer itself but the ratio $d_{a\text{-}Si:H}/L_D^{aSi:H}$ that appears in the θ_1 and θ_2 correction factors. By reducing the Debye length (corresponding to a higher DOS at the Fermi level in a-Si:H according to Eq. (5)), one can diminish the effect implied by the finite thickness of the (p) a-Si:H layer compared to the infinite case. An example for $\Delta E_V = 0.5$ eV is given in Fig. 11.

One can see that increasing $N(E_F)$ by one order of magnitude from 10^{19} to 10^{20} cm^{-3} eV^{-1} brings the apparent diffusion potential back to the values calculated for the semi-infinite (p) a-Si:H case thus canceling the effect caused by the limited thickness of 10 nm. Once the Debye length becomes significantly smaller than the thickness of the (p) a-Si:H layer, the metal/a-Si:H and a-Si:H/c-Si interfaces are decoupled and the band bending at the a-Si:H/c-Si interface along with the capacitance behavior are the same as for a semi-infinite a-Si:H layer.

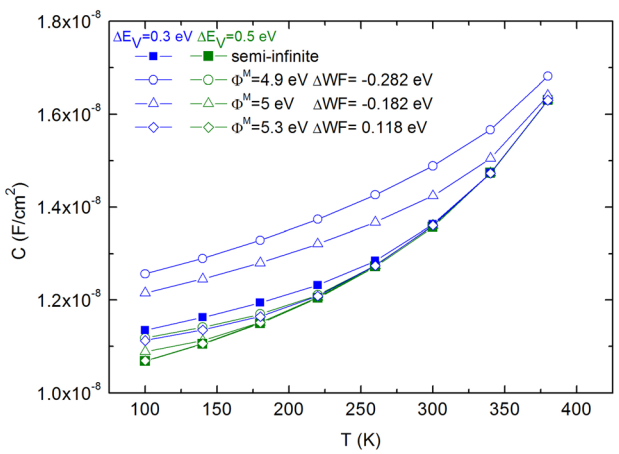


FIG. 10. Comparison of the capacitance-temperature dependencies for different values of the metal work function, $q\Phi^M$, for $d_{a\text{-}Si:H} = 10$ nm and for two values of valence band offset ($\Delta E_V = 0.3$ eV and 0.5 eV).

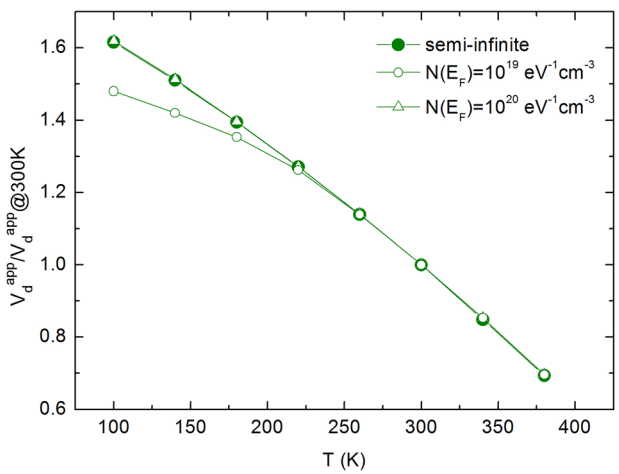


FIG. 11. Influence of the density of states at the Fermi level, $N(E_F)$, in a 10 nm thick (p) a-Si:H on the normalized apparent diffusion potential evolution with temperature for $\Delta E_V = 0.5$ eV. The metal work function is 4.9 eV.

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3. Combined influence of the finite thickness of the (p) a-Si:H layer and of the (i) a-Si:H buffer layer

In Secs. C.1 and C.2, we have shown how the temperature dependence of the quasistatic capacitance was affected by either the insertion of a thin (i) a-Si:H buffer layer, the (p) a-Si:H layer being semi-infinite, or the finite thickness of the (p) a-Si:H layer together with the work function of the contact electrode, without (i) a-Si:H buffer layer. In this section, we study the combined effect of the (i) a-Si:H buffer layer and the finite thickness of the (p) a-Si:H layer in order to go toward real solar cell structures. The results are shown in terms of normalized apparent diffusion potential in Fig. 12. We chose a large value of the valence band offset ($\Delta E_V = 0.5$ eV) where the strong inversion layer is present in the whole temperature range for semi-infinite (p) a-Si:H layer without (i) a-Si:H buffer layer. Again we observe that the insertion of a 10 nm thick a-Si:H buffer layer only slightly impacts the curve at very low temperature ($T < 150$ K). If we do not introduce the buffer layer but introduce a finite (p) a-Si:H thickness of 10 nm, the weaker temperature dependence indicating that the strong inversion condition in c-Si is lost can be seen here below 250 K for the electrode work function taken at 4.9 eV. Finally, if we introduce both the (i) a-Si:H buffer layer and the finite (p) a-Si:H thickness, we can observe that the temperature range with weaker slope is extended further ($T < 300$ K). These trends can be explained from Eq. (41). Indeed, for the values of the work function and the densities of states in (i) a-Si:H and (p) a-Si:H considered here, we have $0 < \theta_1 < 1$, and the two correcting terms in the left hand side of Eq. (41) are negative. This leads to a cumulative effect of the (i) layer and finite (p) layer in increasing the value of $u_e(0)$ which extends to higher temperature the range where strong inversion has disappeared.

D. Comparison with experimental results

Having developed the theoretical calculation of the temperature dependence of the quasistatic capacitance we aim at comparing it with experimental data measured on high efficiency silicon heterojunction solar cells in order to get insight into the electrical device parameters like the valence band offset, and the work function of the contacting electrode at the (p) a-Si:H side.

The measured solar cells were provided by EPFL and INES-CEA. These were high efficiency solar cells (AM1.5 efficiency of about 22% with open-circuit values of around 730 mV) that were fabricated on n-type crystalline silicon of doping density around 10^{15} cm^{-3}.[3,26] The capacitance was measured using Agilent 4284A and E4980A precision LCR meters at different DC biases (from -2 V to $+0.5$ V) and frequencies (20 Hz–1 MHz) in the temperature range 90 K–420 K. Very similar results were obtained on the solar cells from both institutes. Here, we will use the experimental data obtained on cells from EPFL. Details on the preparation of these cells are provided in Ref. 3. The front emitter junction consists of a (p) a-Si:H/(i) a-Si:H stack with thicknesses of 10 and 5 nm for the doped and undoped layers, respectively. These values were fixed for all following calculations. The top contact electrode is made of indium tin oxide (ITO) (partially covered by a silver grid that does not play a role in the capacitance). The back contact is made of a (n) a-Si:H/(i) a-Si:H/ITO/Ag stack that should have no influence on the temperature dependence of the device capacitance.

From a previous analysis of planar conductance measurements on a-Si:H/c-Si heterostructures, we obtained that the valence band offset was close to 0.4 eV,[13] while an average value of 0.46 eV was reported from photoelectron spectroscopy.[27] Thus, in our calculations, we varied the valence band offset between 0.4 and 0.5 eV. Results of our calculations are compared to experimental data in Figs. 13 and 14 for $\Delta E_V = 0.4$ eV and $\Delta E_V = 0.5$ eV, respectively. Note that the normalization of experimental values of capacitance or apparent diffusion potential to that at 300 K is interesting to get rid of the value of the junction area that may not be known very precisely due to the texturization of the surface. This comparison shows that the experimental data can be well reproduced by the calculations and that there is not a

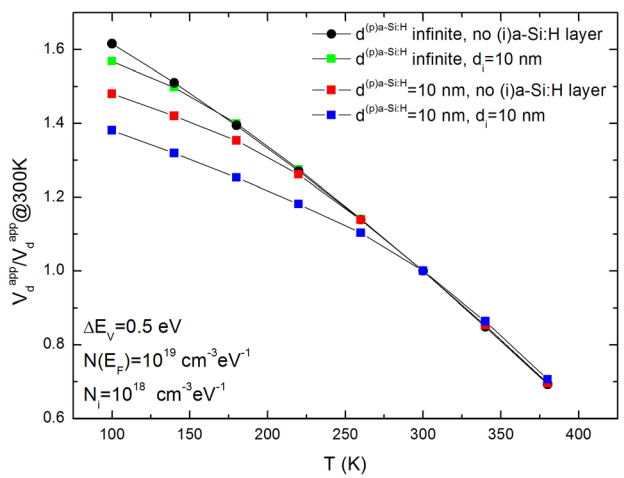


FIG. 12. Comparison of the temperature dependence of the normalized apparent diffusion potential for different cases: no (i) a-Si:H layer and semi-infinite (p) a-Si:H, 10 nm thick (i) a-Si:H layer and semi-infinite (p) a-Si-H, no (i) a-Si:H layer and 10 nm thick (p) a-Si:H layer, 10 nm thick (i) a-Si:H layer and10 nm thick (p) a-Si:H layer. Standard parameters of Table I were used with $\Delta E_V = 0.5$ eV, $N_i = 10^{18}$ cm^{-3} eV^{-1}, $\Delta E_F = 0.65$ eV, and $q\Phi^M = 4.9$ eV.

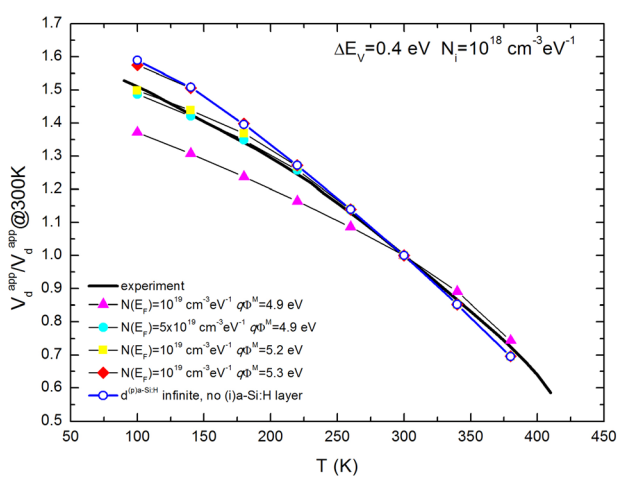


FIG. 13. The experimental temperature dependence of the apparent voltage drop normalized to its value at 300 K is compared with calculations with a valence band offset of 0.4 eV and different sets of other parameters.

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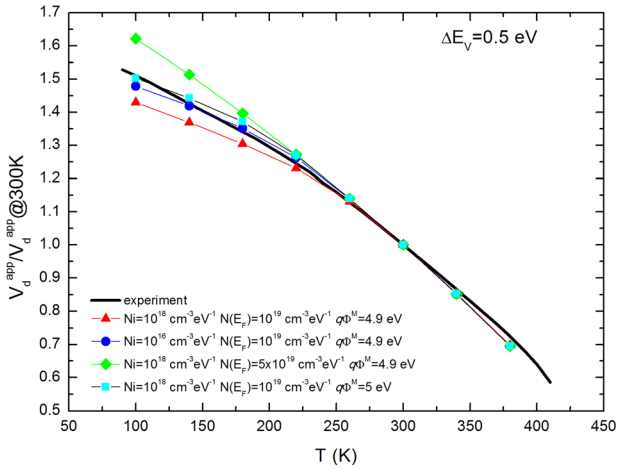


FIG. 14. The experimental temperature dependence of the apparent voltage drop normalized to its value at 300 K is compared with calculations with a valence band offset of 0.5 eV and different sets of other parameters.

unique set of parameters that provides a good reproduction of these data as discussed below.

In Fig. 13, where we fixed $\Delta E_V = 0.4\,\text{eV}$, we can observe that an almost equivalent good reproduction of experimental data is obtained for two couples of $N(E_F)$ and metal work function $(q\Phi^M)$: $N(E_F) = 5 \times 10^{19}\,\text{cm}^{-3}\,\text{eV}^{-1}$ and $q\Phi^M = 4.9\,\text{eV}$ on one hand, and $N(E_F) = 1 \times 10^{19}\,\text{cm}^{-3}\,\text{eV}^{-1}$ and $q\Phi^M = 5.2\,\text{eV}$ on the other hand. This can be easily understood from our previous discussion of the effect of the work function of the contact electrode. Indeed, the experimental temperature dependence of the normalized apparent diffusion voltage exhibits a small flattening of the slope at low temperature ($T < 200\,\text{K}$) compared to what would be obtained for a semi-infinite (p) a-Si:H layer. This means that the strong inversion layer is not so strong as it would be for a semi-infinite (p) a-Si:H layer and it tends to disappear at low temperature. This can be obtained from a counter band-bending coming from the contact electrode, implying a negative ΔWF value. We first fixed $N(E_F)$ at $1 \times 10^{19}\,\text{cm}^{-3}\,\text{eV}^{-1}$. It can be seen in Fig. 13 that if we progressively lower $q\Phi^M$ (thus rendering ΔWF more negative), the curve is flattened at low temperature. The flattening is not sufficient to match with the experimental data for $q\Phi^M = 5.3\,\text{eV}$, it is well adapted for $q\Phi^M = 5.2\,\text{eV}$ and becomes too pronounced for $q\Phi^M < 5\,\text{eV}$. If the DOS in (p) a-Si:H is larger, the effect of the contact electrode is more shielded and this requires to use a lower value of $q\Phi^M$ (larger negative ΔWF) to obtain the same effect. This is why, for $N(E_F) = 5 \times 10^{19}\,\text{cm}^{-3}\,\text{eV}^{-1}$, we need to decrease $q\Phi^M$ to 4.9 eV to obtain an almost equivalent good reproduction of the experimental data as obtained with $q\Phi^M = 5.2\,\text{eV}$ for $N(E_F) = 1 \times 10^{19}\,\text{cm}^{-3}\,\text{eV}^{-1}$.

If we fix $\Delta E_V = 0.5\,\text{eV}$, the inversion layer will be stronger compared to $\Delta E_V = 0.4\,\text{eV}$ if all other parameters are kept identical. Therefore, as can be seen in Fig. 14, we need to reinforce the effect of the counter band-bending coming from the contact electrode in order to reproduce the experimental data at low temperature. This is why the couple $N(E_F) = 5 \times 10^{19}\,\text{cm}^{-3}\,\text{eV}^{-1}$ and $q\Phi^M = 4.9\,\text{eV}$ that was able to reproduce the experimental data for $\Delta E_V = 0.4\,\text{eV}$ does not provide enough flattening at low temperature with $\Delta E_V = 0.5\,\text{eV}$. For our nominal input parameters $N(E_F) = 1 \times 10^{19}\,\text{cm}^{-3}\,\text{eV}^{-1}$ and $N_i = 10^{18}\,\text{cm}^{-3}\,\text{eV}^{-1}$, we need to decrease $q\Phi^M$ to 5 eV (as compared to $q\Phi^M = 5.2\,\text{eV}$ for $\Delta E_V = 0.4\,\text{eV}$) in order to reproduce the experimental data. Finally, in Fig. 14, we also show that we need to reinforce the counter-electrode effect by further decreasing $q\Phi^M$ if the DOS in the (i) a-Si:H layer is smaller. Thus, $q\Phi^M = 4.9\,\text{eV}$ also provides a good reproduction of the experimental data if N_i is decreased to $10^{16}\,\text{cm}^{-3}\,\text{eV}^{-1}$.

While the uncertainty in the DOS parameters in (p) a-Si:H and in (i) a-Si:H and in the valence band offset leads to various possible combinations that can equally well reproduce the experimental data, from our analysis of the effect of the finite thickness of the (p) a-Si:H layer combined with the ITO electrode we can however exclude too low values of the ITO work function. There are many reports on the work function of ITO in literature, and the values are widely spread between 4 eV and more than 5.5 eV depending on the deposition conditions, surface treatment, and also depending on the measurement method.[28–30] From the temperature dependence of the capacitance, we could investigate on the contact electrode work function directly at the device level. In our analysis, if $q\Phi^M$ is decreased below 4.7 eV, the absolute values of V_d^{app} become much too low compared to the experimental ones and the temperature dependence becomes almost linear in the whole temperature range. This is because for such low values of $q\Phi^M$ the strong hole inversion layer at the c-Si surface disappears in the whole temperature range, while our experimental capacitance data give clear evidence to the presence of the strong inversion layer above 250 K.

IV. CONCLUSIONS

The complete analytical calculation of capacitance that takes into account the contribution of holes in (n) c-Si was developed in order to reproduce the increase with temperature of the capacitance measured on (p) a-Si:H/(n) c-Si heterojunction solar cells. It was shown that this increase is stronger than expected from the classical depletion layer capacitance due to a strong inversion layer that exists at the interface of (p) a-Si:H/(n) c-Si. The full analytical calculation allows one to consider the contribution of the holes to the space charge density and calculate independently the depletion charge and the charge of holes in (n) c-Si. It was shown that within the complete analytical approach the strong inversion layer is promoted with temperature and brings significant increase to the capacitance for moderate and large values of the valence band offset ($\Delta E_V > 0.3\,\text{eV}$).

The influence of the (i) a-Si:H buffer layer at a-Si:H/c-Si interface on the calculation of the capacitance and its evolution with temperature was considered. Compared to the semi-infinite a-Si:H case, the introduction of the (i) a-Si:H layer leads to a decrease of band bending in c-Si. This decrease is enhanced if the thickness of the (i) layer or if the density of states in this layer increases. This can result in the suppression of the strong inversion layer at the c-Si surface,

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which can be evidenced by the appearance of a weaker temperature dependence of the capacitance.

The finite thickness of (p) a-Si:H layer was introduced into calculations as well. The effect of this finite thickness depends on the work function of the contact electrode and on the DOS in (p) a-Si:H. If the work function of the contact electrode is lower than that of (p) a-Si:H, a Schottky barrier develops at the contact electrode. This counter-diode can also lead to a decrease of the band bending in c-Si, again potentially leading to the suppression of the strong inversion at the c-Si surface as evidenced by the weaker temperature dependence of the capacitance. The finite thickness effect also depends on the DOS in (p) a-Si:H, since increasing the DOS can shield the counter-diode band bending.

At last, we used the previously described observations to fit the experimental data obtained on high efficiency solar cells. The temperature dependence of the low frequency capacitance clearly evidences the existence of strong inversion conditions at the c-Si surface for temperatures above 250 K. At lower temperatures, the weaker temperature dependence observed is a signature of the disappearance of strong inversion. A good reproduction of these experimental data can be obtained for $\Delta E_V = 0.4 - 0.5$ eV with reasonable DOS values in a-Si:H and ITO work function values ranging between 4.7 and 5.1 eV.

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APPENDIX: CALCULATION OF THE CHARGES FOR THE CASE WITH THE FINITE THICKNESS OF THE (p) a-Si:H LAYER AND (i) a-Si:H BUFFER LAYER

Introduction of a finite thickness of the (p) a-Si:H layer, $d_{a\text{-}Si:H}$, and of a thin (i) a-Si:H buffer layer of thickness d_i requires the modification of the charge neutrality condition where the terms related to the charge on the electrode on the p-side of the heterojunction, $Q^{electrode}$, and that of the (i) a-Si:H layer adds a term, $Q^{(i)a\text{-}Si:H}$ have to be added

$$Q^{(p)a-Si:H} + Q^{(i)a-Si:H} + Q^{electrode} + Q^{c-Si} = 0. \quad \text{(A1)}$$

The space charge density in (i) a-Si:H, for $-d_i \le x \le 0$ ($x = 0$ corresponding to the (i) a-Si:H/(n) c-Si interface), is written

$$\rho(x) = q^2 N_i[(V(-\infty) - V(x) + \Delta E_F/q)], \quad \text{(A2)}$$

with

$$\Delta E_F = (E_{FB}^i - E_V^i) - (E_{FB}^p - E_V^p) - \Delta E_V^{p/i}, \quad \text{(A3)}$$

where N_i is the density of states in (i) a-Si:H taken here constant within the bandgap, ${E_{FB}}^i - {E_V}^i$ and ${E_{FB}}^p - {E_V}^p$ are the positions of the Fermi level with respect to the valence band edge that ensure charge neutrality in the (i) and (p) a-Si:H layers (i.e., the values that would prevail in a bulk material), respectively, $\Delta {E_V}^{p/i}$ is the valence band offset at the (p) a-Si:H/(i) a-Si:H interface (such an offset could appear due to the high doping effects and different hydrogen content in the (p) a-Si:H compared to (i) a-Si:H; furthermore the (i) a-Si:H layer could be replaced by another material like an oxide layer so that $\Delta {E_V}^{p/i}$ more generally stands for the valence band offset between the doped a-Si:H and the interface buffer layer).

The space charge density in (p) a-Si:H, for $-d_i - d_{a\text{-}Si:H} \le x \le -d_i$, is written

$$\rho(x) = q^2 N(E_F)^{a-Si:H}[V(-\infty) - V(x)]. \quad \text{(A4)}$$

Then solving Poisson's equation, one can obtain the following expression for the electric field in the (i) buffer layer:

$$L_i E(x) = -\left[V(0) - V(-\infty) - \Delta E_F/q\right] \frac{\cosh\frac{x+d_i}{L_i}}{\sinh\frac{d_i}{L_i}} + \left[V(-d_i) - V(-\infty) - \Delta E_F/q\right] \frac{\cosh\frac{x}{L_i}}{\sinh\frac{d_i}{L_i}}, \quad \text{(A5)}$$

where L_i is the Debye length in (i) a-Si:H

$$L_i = \sqrt{\frac{\varepsilon}{q^2 N_i}}, \quad \text{(A6)}$$

while the electric field in the (p) a-Si:H layer can be obtained from

$$L_D^{a-Si:H} E(x) = -\left[V(-d_i) - V(-\infty)\right] \times \frac{\cosh\frac{x+d_i+d_{a-Si:H}}{L_D^{a-St:H}}}{\sinh\frac{d_{a-Si:H}}{L_D^{a-Si:H}}} + \left[V(-d_i - d_{a-Si:H}) - V(-\infty)\right] \frac{\cosh\frac{x+d_1}{L_i}}{\sinh\frac{d_{a-Si:H}}{L_D^{a-Si:H}}}, \quad \text{(A7)}$$

with

$$V(-d_i - d_{a-Si:H}) - V(-\infty) = \Phi^{a-Si:H} - \Phi^M = \Delta WF. \quad \text{(A8)}$$

From the continuity of the electric field at $x = -d_i$, one can express $V(-d_i) - V(-\infty)$ as a function of $V(0) - V(-\infty)$. Finally, Eq. (A1) is equivalent to expressing the continuity of the electric field at $x = 0$, and this leads to

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$$\frac{qV_d - qV_a - k_BT\left(u_e(\infty) - u_e(0)\right)}{L_D^{a-Si:H}}\theta_1 - \frac{\Delta E_F}{L_D^{a-Si:H}}\theta_2 + \frac{\Delta WF}{L_D^{a-Si:H}}\theta_3 = \frac{k_BT}{L_D^{c-Si}}\sqrt{f\left(u_e(0), V_a\right)}, \tag{A9}$$

where θ_1, θ_2, and θ_3 are correction terms that are given by

$$\theta_1 = \frac{\cosh\left(\frac{d_i}{L_i}\right) + \frac{L_D^{a-Si:H}}{L_i}\sinh\left(\frac{d_i}{L_i}\right)\tanh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right)}{\tanh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right)\cosh\left(\frac{d_i}{L_i}\right) + \frac{L_i}{L_D^{a-Si:H}}\sinh\left(\frac{d_i}{L_i}\right)}, \tag{A10}$$

$$\theta_2 = \frac{\cosh\left(\frac{d_i}{L_i}\right) + \frac{L_D^{a-Si:H}}{L_i}\sinh\left(\frac{d_i}{L_i}\right)\tanh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right) - 1}{\tanh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right)\cosh\left(\frac{d_i}{L_i}\right) + \frac{L_i}{L_D^{a-Si:H}}\sinh\left(\frac{d_i}{L_i}\right)}, \tag{A11}$$

$$\theta_3 = \frac{1}{\sinh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right)\cosh\left(\frac{d_i}{L_i}\right) + \frac{L_i}{L_D^{a-Si:H}}\sinh\left(\frac{d_i}{L_i}\right)\cosh\left(\frac{d^{a-Si:H}}{L_D^{a-Si:H}}\right)}. \tag{A12}$$

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