HardBlare: a Hardware-Assisted Approach for Dynamic Information Flow Tracking
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HardBlare proposes a software/hardware codesign methodology to ensure that security properties are preserved all along the execution of the system but also during files storage. The general context is to address Dynamic Information Flow Tracking (DIFT) that generally consists in attaching marks (also known as tags) to denote the type of information that are saved or generated within the system.

Let’s suppose that “print” function is public and the tag of a variable \( x \) is underlined variable \( x \).

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**Example code**

```c
#include <stdio.h>

int main()
{
    int p = 3; int s = 42; int x = p + s;
    // x = p + s;
    if (x != public)
        print(x);
    if (x != secret)
        print(x);
    return 0;
}
```

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### Advantages
- Flexible security policies
- Overhead (from 300% to 3700%)

### Disadvantages
- Hardware
- Low overhead (<10%)
- Invasive modifications
- Fixed security policies

### In-core DIFT
- Low overhead (<10%)
- Invasive modifications

### Dedicated CPU for DIFT
- Low overhead (<10%)
- Wasting resources
- Few modifications to CPU
- Energy consumption (x 2)

### Dedicated DIFT Coprocessor
- Low overhead (<10%)
- Coprocessor

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**Definitions**

- **Tag dependencies**: block contains annotations loaded when the program is launched.
- **Memory tags**: block contains tags related to information containers.
- **Tag register file**: contains tags related to CPU registers.

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**State of the art**

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<tr>
<th>Software</th>
<th>Hardware</th>
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<tr>
<td>Flexible security policies</td>
<td>Overhead (from 300% to 3700%)</td>
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<td>Multiple attacks detected</td>
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<tr>
<td>Low overhead (&lt;10%)</td>
<td>Low overhead (&lt;10%)</td>
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<td>Invasive modifications</td>
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<td>Energy consumption (x 2)</td>
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<td>Low overhead (&lt;10%)</td>
<td>Low overhead (&lt;10%)</td>
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<tr>
<td>Communication between CPU and DIFT Coprocessor</td>
<td>Coprocessor</td>
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**Static Analysis**

- During the compilation phase, a static analysis is done on the LLVM intermediate representation produced from the source code, and propagated to the ARM backend for the machine code generation.
- The result of static analysis gives a list of dependencies between information containers (e.g., registers, memory spaces...) for every basic blocks which are stored on a dedicated section in a ELF File.
- During run-time, the Program Trace Macrocell (PTM) generates a trace containing the address for each committed instruction modifying the PC value.
- Annotations related to the basic block identified by its address, given by the trace, are processed by the coprocessor to propagate tags.

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**DIFT step-by-step**

- ARM CoreSight Components export trace (for both CPUs) towards PL in PFT (Program Flow Trace) protocol.
- PFT Decoder decodes trace in usable format.
- Using decoded trace, DIFT Coprocessor reads tags dependencies block.
- DIFT Coprocessor looks for the tags either in memory or tag register file.
- DIFT Coprocessor computes tags depending on propagation rules.
- DIFT Coprocessor updates corresponding tags.
- DIFT Coprocessor checks for security policy violation and raise an interruption.

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**ARM Cortex-A9 Trace mode: Coresight components**

- Source code compiler.
- LLVM IR.
- Static Analysis.
- ELF File.
- Operating System (kBlare).
- ARM Co-Processor.
- ARM Cortex-A9 CoreSight Debug Trace.
- ARM CoreSight Multicore Debug & Trace.
- FPGA Programmable Logic (PL).
- Processor System (PS).
- DIFT Coprocessor.
- PFT Decoder.
- Tag Register File.
- Memory Tags.
- Tag Dependencies.
- Traces.

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**Main Contributions at a Glance**

- Hardware-assisted DIFT system with limited time overheads.
- Approach based on a non-modified CPU with a standard Linux and generic binaries. Could be implemented by industrial partners in medium-term.
- Hardened with hardware security mechanisms: trusted coprocessor storage and bus protection in terms of confidentiality/integrity.
- Contributions on software-related issues as well (static/dynamic IFC analysis, i.e. hybrid analysis).
- Perspectives on runtime reconfiguration and multicore/manycore systems.

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**Some References**