HardBlare: a Hardware-Assisted Approach for Dynamic Information Flow Tracking
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### Introduction

HardBlare proposes a software/hardware codesign methodology to ensure that security properties are preserved all along the execution of the system but also during files storage. The general context is to address **Dynamic Information Flow Tracking (DIFT)** that generally consists in attaching marks (also known as tags) to denote the type of information that are saved or generated within the system.

Let's suppose that “print” function is public and the tag of a variable x is underlined variable x.

<table>
<thead>
<tr>
<th>Example code</th>
<th>Tag initialization</th>
<th>Tag propagation</th>
<th>Tag check</th>
</tr>
</thead>
<tbody>
<tr>
<td>p = 3;</td>
<td>p ← public</td>
<td></td>
<td></td>
</tr>
<tr>
<td>α = 42;</td>
<td>s ← secret</td>
<td></td>
<td></td>
</tr>
<tr>
<td>x = α + p + s;</td>
<td>x ← p + s</td>
<td></td>
<td></td>
</tr>
<tr>
<td>print(x);</td>
<td></td>
<td>if (x != public)</td>
<td>raise interruption</td>
</tr>
</tbody>
</table>

### State of the art

<table>
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<th>Hardware</th>
<th>Advantages</th>
<th>Disadvantages</th>
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<tr>
<td>DIFT</td>
<td>Flexible security policies</td>
<td>Overhead (from 300% to 3700%)</td>
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<tr>
<td>In-core</td>
<td>Low overhead (&lt;10%)</td>
<td>Invasive modifications</td>
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<tr>
<td>Dedicated CPU for DIFT</td>
<td>Low overhead (&lt;10%)</td>
<td>Wasting resources</td>
</tr>
<tr>
<td>Dedicated DIFT Coprocessor</td>
<td>Low overhead (&lt;10%)</td>
<td>Energy consumption (x 2)</td>
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<td></td>
<td>Flexible security policies</td>
<td>Communication between CPU and DIFT</td>
</tr>
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</table>

### Dynamic Information Flow Tracking

- During the compilation phase, a static analysis is done on the LLVM intermediate representation produced from the source code, and propagated to the ARM backend for the machine code generation
- The result of static analysis gives a list of dependencies between information containers (e.g. registers, memory spaces...) for every basic blocks which are stored on a dedicated section in a ELF File
- During run-time, the Program Trace Macrocell (PTM) generates a trace containing the address for each committed instruction modifying the PC value
- Annotations related to the basic block identified by its address, given by the trace, are processed by the coprocessor to propagate tags

### ARM Cortex-A9 Trace mode: Coresight components

**Definitions**
- **Tag dependencies** block contains annotations loaded when the program is launched
- **Memory tags** block contains tags related to information containers
- **Tag register file** contains tags related to CPU registers

**DIFT step-by-step**
- ARM CoreSight Components export trace (for both CPUs) towards PL in PFT (Program Flow Trace) protocol
- PFT Decoder decodes trace in usable format
- Using decoded trace, DIFT Coprocessor reads tag dependencies block
- DIFT Coprocessor looks for the tags either in memory or tag register file
- DIFT Coprocessor computes tags depending on propagation rules
- DIFT Coprocessor updates corresponding tags
- DIFT Coprocessor checks for security policy violation and raise an interruption

### Main Contributions at a Glance

- **Hardware-assisted DIFT system with limited time overheads.**
- **Approach based on a non-modified CPU with a standard Linux and generic binaries**
  - Could be implemented by industrial partners in medium-term.
- **Hardened with hardware security mechanisms: trusted coprocessor storage and bus protection in terms of confidentiality/integrity.**
- **Contributions on software-related issues as well (static/dynamic IFC analysis, i.e. hybrid analysis).**
- **Perspectives on runtime reconfiguration and multicore/manycore systems.**

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