0.18-μm CMOS Driver Optimization for Maximum Data Rate under Power and Area Constraints

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***Abstract*—This paper presents a Mach-Zehnder-based transmitter in 0.18 µm CMOS. An asymmetric driver is proposed to achieve a large output swing on the optical modulator. The logical effort method was applied on each driver block in order to optimize the propagation delay. The driver characteristics are analyzed based on slew-rate limitation. The speed-power-area trade-off is highlighted and enables to adjust the driver design according to specified constraints. Driver performance obtained with early-design-stage equations is compared to post-layout simulations. Good agreement is demonstrated which validates the proposed sizing methodology.**

Keywords—Mach-Zehnder driver; logical effort; power-speed-area trade-off

I. INTRODUCTION

Silicon photonics is considered as a prime technology for communication and high-speed computing applications. Indeed photonic devices offer promising solutions for next-generation high-speed and high-density interconnects. Mach-Zehnder-based transmitters have been proposed to implement cost-effective and energy-efficient optical links in order to meet power and bandwidth datacoms standards [1, 2].

This work reports on the optimization of a silicon photonics transmitter based on a Mach-Zehnder interferometer and an asymmetric driver. We focuses particularly on the driver design which is demonstrated in a low-cost 0.18 µm CMOS process. The driver has to address the maximum data rate while ensuring low- power and area constraints.

Driver circuitry is often designed in the literature [2], [3], [4], however transistors' sizing is rarely revealed. Our approach is based on the logical effort method. To the authors' knowledge, such an approach is reported in a paper for the driver design for the first time. The logical effort method enables designers to optimize digital circuits for speed [5]. It shows how to reduce the overall delay and how to find the ideal number of gates in a logic chain. As a result, the fastest implementation of any given logic function is pointed out.

This paper demonstrates that early-design-stage equations are quite accurate to derive driver performance. Equations show good agreement with post-layout simulation results. The paper is organized as follows. Section II reviews the Mach-Zehnder modulator operation. In section III, the driver architecture is described. The driver sizing is introduced by the means of the logical effort methodology. Following subsections discuss the trade-off between speed, power, and area which permits to design the driver to the targeted application. Section IV presents electrical and post-layout simulation results and summarizes driver performance along with comparison to analytic equations. Finally, Section V concludes the paper.

II. PHOTONICS APPLICATION

The architecture of a simplified Mach-Zehnder-based modulator is depicted in Fig. 1. It consists of an input waveguide, a splitter, two Mach-Zehnder arms and an output combiner. The splitter and the combiner are implemented with optical directional couplers and a phase shifter is integrated in one of the two arms. Another phase shifter is usually introduced in the second arm to obtain same optical losses, keeping a zero phase shift [1]. The Mach-Zehnder interferometer enables to convert a phase modulation into an intensity modulation by recombining two light beams with different phases.

The variation of free carrier concentration is used to induce a modulation in the silicon. This variation creates a change in the optical index of the material which results in a phase shift of the light wave. In order to realize such a phase shifter, a PN diode is inserted into the arm of a Mach-Zehnder interferometer. When reversed biased, the diode enters in carrier depletion mode. This expands the space charge region and thus changes the carrier concentration. The bias is applied to the diode via the *Driver Cathode* of Fig. 1.

One can show that it is interesting to bias the PN junction not only in reverse but also in forward. Forward bias is made with the *Driver Anode* illustrated in Fig. 1. This solution benefits from a larger voltage swing on the modulator. However the forward bias must remain below the built-in potential to ensure that the diode does not enter in the carrier injection mode. The

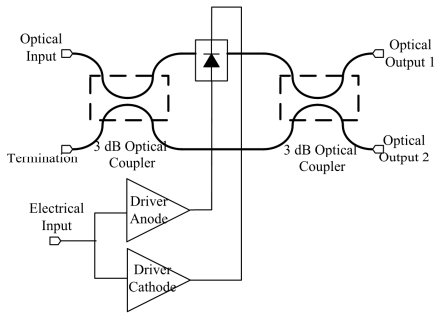

Fig. 1. Mach-Zehnder modulator architecture.

built-in potential is around 0.5 V depending on the junction doping.

From a device point of view, the lateral PN junction is defined in the center of a rib waveguide. A silicon layer of 300 nm thickness is formed with P and N implants as shown in the schematic cross section of Fig. 2 (a). AC simulations are performed in order to extract the capacitance of the device. C-V curve is illustrated in Fig. 2 (b) and exhibits a 300 fF capacitance for a 1mm long PN diode.

To connect the drivers to the diode, different integration technics can be considered. The literature reports mainly two methods: either the monolithic [2, 4] or the hybrid integration [3]. When monolithically integrated, photonic and electronic components are fabricated into the same CMOS node. On the contrary, hybrid integration benefits from separate optimization of Mach-Zehnder modulator and drivers. Electro-optic transmitter design requires to focus on this issue, however following sections will take an interest only on driver circuitry.

III. Driver Optimization

This work aims to develop a driver for a Mach-Zehnder-based modulator in a 0.18 µm CMOS node. The driver design is optimized for the minimum propagation delay. The driver characteristics are then analyzed to verify if they satisfy data rate, power and area constraints.

A. Driver circuits

The driver architecture is inspired from the asymmetric driver used in [3]. It is composed of two distinct blocks, the *Driver Anode* and the *Driver Cathode* that drive respectively the anode and the cathode of the modulator's PN junction. The maximum voltage swing from 0 to V_{DD} is allowed on the cathode whereas the forward bias on the anode has to be limited below the built-in potential.

The *Driver Cathode* enables to shape input signals and to drive high capacitive load. Its topology uses a chain of four inverters, namely (M_{p1}; M_{n1}) to (M_{p4}; M_{n4}). Following subsection highlights the transistors' sizing in order to optimize the propagation delay.

The *Driver Anode*'s purpose is similar to those of *Driver Cathode*. Its topology is also based on an inverter chain but an additional circuit enables to reduce the high voltage level under the built-in potential. Fig. 3 shows the driver circuit. The main inverter chain is composed by the transistors M_{n1}, M_{p1}, M_{n2}, M_{p2}, M_{n3}, and M_{p3}. In order to be able to control precisely the voltage applied on the PN junction, the *controller circuit* formed by the two inverters M_{n4}, M_{p4} and M_{n5}, M_{p5} and by the PMOS transistor M_{p6} is introduced. This circuit enables to activate or deactivate the transistor M_{n6} working as a switch. M_{n6} is switched on when

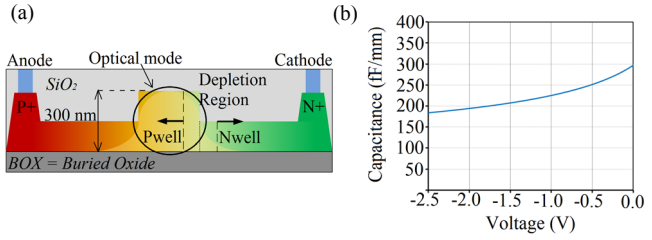

Fig. 2. (a) PN diode cross section; (b) Junction capacitance versus reverse bias.

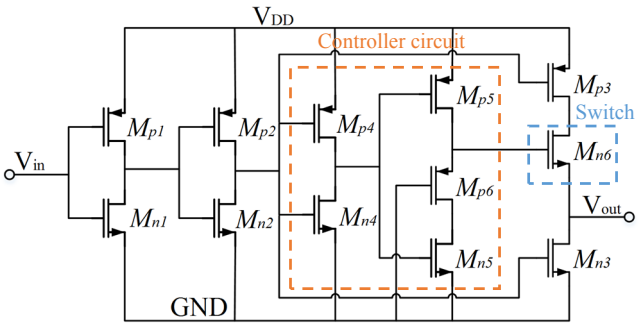

Fig. 3. Driver Anode: transistor-level schematics.

M_{p3} is activated, then the *controller circuit* switches M_{n6} off in order to limit the high level to a value close to the built-in potential.

B. Transistors sizing: the logical effort method

The logical effort method was introduced in [5] in order to help designers to optimize any logic circuits for speed. When adapted to an inverter chain, the method leads to a sizing methodology to find both the ideal number of stages and all gates' sizes. In this section a sizing approach is proposed in order to minimize the drivers' propagation delays. The starting assumption is based on the knowledge of the output load that the driver must drive. Besides, all transistors gate lengths are imposed to be equal to the minimum L_{min}.

When considering a multi-stage logic network, the first step consists in computing the product $F = GBH$ called the path effort. G is the path electrical effort and captures the effect of each gate's topology on its capability to produce output current. In the case of inverters, G is one. B is the path branching effort and enables to take into account the fan-out of the gates' chain. B is also one for proposed drivers. H is the path electrical effort and describes how the electrical environment of the circuit affects its performance. H is equal to $\frac{C_{mod}}{C_{in}}$ where C_{mod} is the load of the last stage, i.e. the modulator capacitance. C_{in} is the input capacitance of the first stage which can be calculated from the gate oxide area capacitance C_{ox}. As a consequence, the path effort is:

$$F = H = \frac{C_{mod}}{C_{ox} L_{min} (W_{n,1} + W_{p,1})} \quad (1)$$

Then the optimal number of inverters stages can be estimated by the following expression:

$$N_{opt} = \frac{\ln(F)}{\ln(\rho)}, \quad (2)$$

where the optimum stage effort ρ is defined as the solution of the equation $\rho\,(1 - \ln(\rho)) + p_{inv} = 0$ and p_{inv} is the parasitic delay of an inverter. p_{inv} has a fixed value independent of the gate's size and of its output load. The best number of stages N is then the next integer above N_{opt}.

The logical effort method shows that the propagation delay is minimized when each stage in the path bears the same stage effort f which results in:

$$f = F^{\frac{1}{N}} \tag{3}$$

In the case of an inverter chain, the stage effort f is the ratio between inverters sizes. As a result, the transistors' sizing is easily made such as:

$$\begin{cases} W_{n,i} = f\, W_{n,(i-1)} & \forall i = 1 \dots N \\ W_{p,i} = \beta\, W_{n,i} \end{cases} \tag{4}$$

The factor β is introduced in order to achieve equal rising and falling times. Finally the propagation delay between the first and the last stage is derived according to:

$$Delay = \tau\, N\, (f + p_{inv})\,, \tag{5}$$

where τ is the delay of an ideal inverter that drives the same inverter.

Based on the logical effort method, sizing is carried out on both *Driver Anode* and *Driver Cathode* with a modulator load of 300 fF. The other parameters for the considered CMOS node are $p_{inv} = 2.33$, $\tau = 8\,ps$, $L_{min} = 0.18\,\mu m$ and $C_{ox} = 8.8\,fF/\mu m^2$. The method shows that the optimal number of stages is 2.3. Therefore we choose $N = 3$ for the *Driver Anode* and $N = 4$ for the *Driver Cathode* since the two driver blocks must have a complementary logic function. Transistors' widths are given in Table I. They are calculated using (4) and a factor β equal to 2.5.

Regarding the *Driver Anode*, it remains to size the inverters M_{n4}, M_{p4} and M_{n5}, M_{p5} and the two transistors M_{n6} and M_{p6}. For the inverters, we can also use the logical effort method. Their load capacitance corresponds to the M_{n6} input load which is quite small, so these inverters are relatively small. Transistor M_{n6} width is directly linked to the high level value of the output voltage while the transistor M_{p6} enables to smooth the output signal. Their sizing have been made in order to adjust the output signal to the specifications.

C. *Area and power consumption compromises versus driver speed*

After having sized both drivers, this section describes how to estimate the maximal data rate achievable by each driver and its power consumption. Indeed, the driver optimization leads to trade-off between speed, energy efficiency and area. These characteristics are analyzed below.

We assume that the data rate is limited by the inverters rising and falling times, based on slew-rate calculations of [4]. We consider that the falling time (equal to the rising time) is about half the duration of a bit period. Hence we have $DR = \frac{0.5}{t_f}$. Besides by using the slew rate formula, the falling time is connected to the load capacitance according to:

$$t_f = \frac{V_{DD}}{I_D}\left(C_{mod} + C_{par}\right) \tag{6}$$

where C_{par} is the parasitic capacitance of the last stage of the inverter chain (either *Driver Anode* or *Driver Cathode*). C_{par} takes into consideration the total gate-drain capacitance and the total drain-body capacitance of both NMOS and PMOS transistors. For more convenience, this last expression is rewritten by introducing C_p whose value is 0.9 fF/µm for 0.18µm technological node:

$$C_{par} = C_p\, W_{n,N}\, (1 + \beta) \tag{7}$$

Finally the data rate limitation comes to the following expression where $J_{D,n}$ is the current density of the NMOS transistor:

$$DR = 0.5\,\frac{J_{D,n} W_{n,N}}{V_{DD}\left(C_{mod} + C_p W_{n,N}\,(1+\beta)\right)} \tag{8}$$

The average power consumption can be estimated by considering the sum of the modulator capacitance and of the driver parasitic capacitance:

$$P = \left(C_{mod} + C_p\left(\sum_{i=1}^{N} W_{n,i} + W_{p,i}\right)\right) V_{DD}^2\, DR \tag{9}$$

Eq. (8) reflects the balance between the data rate and an estimation of the area represented by the NMOS width $W_{n,N}$ of the last driver stage. In Fig. 4, the last NMOS width is plotted versus the data rate for $J_{D,n} = 0.38\ mA/\mu m$, $V_{DD} = 1.8\,V$, and $C_{mod} = 300\,fF$. In addition, Eq. (9) explains the power versus data rate trade-off but (9) depends on the number of stages N and on all transistors sizes. That is why an upper and a lower limit of the power consumption is showed in Fig. 4. These limits depend only on the last stage's size and are calculated as:

TABLE I. DRIVER ANODE AND DRIVER CATHODE SIZING

Transistors	Transistors widths in µm for L = 0.18 µm	
	Driver Anode	*Driver Cathode*
(M_{p1} ; M_{n1})	(4.3 ; 1.7)	(4.3 ; 1.7)
(M_{p2} ; M_{n2})	(14 ; 5.5)	(10 ; 4.0)
(M_{p3} ; M_{n3})	(44 ; 17.5)	(25 ; 10)
(M_{p4} ; M_{n4})	(2.5 ; 1.0)	(60 ; 24)
(M_{p5} ; M_{n5})	(4.3 ; 1.7)	-
M_{p6}	3.0	-
M_{n6}	5.0	-

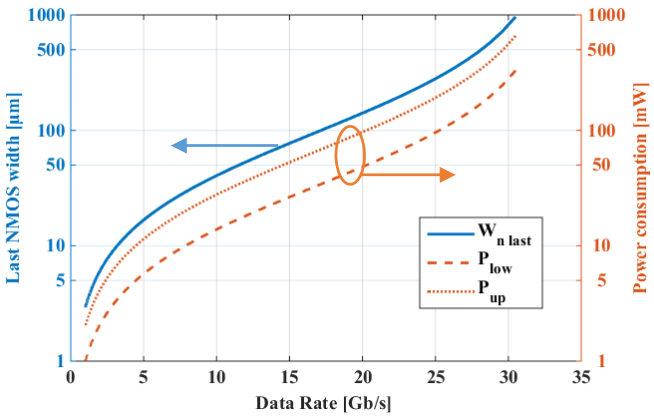

Fig. 4. "Speed-power-area" trade-off: last NMOS width (solid line) and power consumption (dotted and dashed lines) versus data rate

$$P_{up} = V_{DD}\, J_{D,n}\, W_{n,N} \tag{10}$$

$$P_{low} = \left(C_{mod} + C_p W_{n,N}\,(1+\beta)\right) V_{DD}^2\, DR \tag{11}$$

As a result, the two equations (8) and (9) enable us to illustrate the "speed-power-area" compromise for the driver. Thus these equations can be used to adapt the driver to a specific application constrained to data rate, power and area.

IV. Simulation Results

In this section, post-layout simulations are carried out. To this end, driver layouts were done considering RF layout recommendations described in [6]. *Driver Anode* area is 18.8 µm × 39.6 µm. *Driver Cathode* area is 19.2 µm × 39.9 µm. Due to paper space constraints, layout illustrations are not presented here.

A comparison between analytic results and simulation results (electrical and post-layout) is performed. Fig. 5 presents the transient responses of both driver stages. The input signal is in each case a periodic signal from 0 to V_{DD}. The resulting data rate (5Gb/s in Fig. 5(a) and 7Gb/s in Fig. 5(b)) is the maximum for a correct bit transmission. The post-layout output signal is overall not deteriorated in comparison to electrical simulations, validating thus the drivers' layout. The main consequence of parasitic elements consists in increasing the propagation delays. However the *Driver Anode* high level value is also increased which can be problematic if it overpasses the built-in potential of the PN junction. This increase has to be taken into account in further designs.

Finally Tables II and III show an overview of *Driver Anode* and *Driver Cathode* performance. A really good accordance can be noticed between analytic results obtained with equations (5), (8), and (9) and simulations results. Note that for the *Driver Anode*, analytic results are obtained for a three inverters chain without the *controller circuit* and the *switch transistor* while simulations results take into consideration the complete driver.

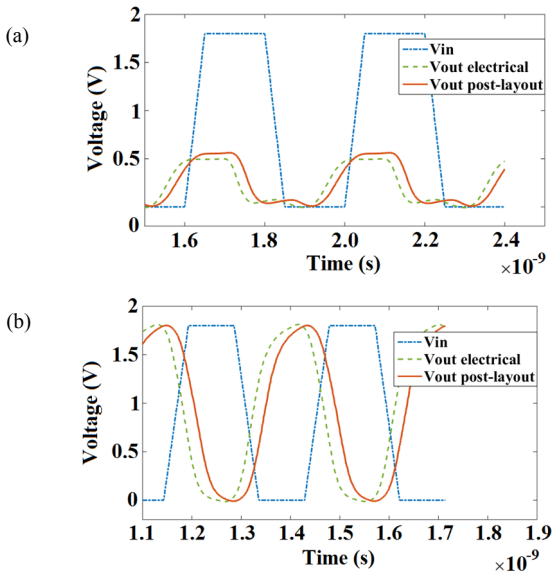

Fig. 5. Transient responses: (a) Driver Anode at 5 Gb/S; (b) Driver Cathode at 7 Gb/s

TABLE II. Driver Anode: performances comparison

ANODE STAGE	Analytic results[a]	Electrical results	Post-layout results
Data rate (Gb/s)	5.2	6	5
Rising / falling times (ps)	96	$t_r = 63$ $t_f = 50$	$t_r = 76$ $t_f = 46$
Propagation delays (ps)	133	$\tau_{PHL} = 107$ $\tau_{PLH} = 128$	$\tau_{PHL} = 132$ $\tau_{PLH} = 158$
Power consumption (mW)	6.4	4.5	4.3
Energy efficiency (pJ/bit)	1.2	0.75	0.86

[a] Analytic results are obtained for a chain of 3 inverters without M_{n4}, M_{p4}, M_{n5}, M_{p5}, M_{n6}, and M_{p6}.

TABLE III. Driver Cathode: performances comparison

CATHODE STAGE	Analytic results	Electrical results	Post-layout results
Data rate (Gb/s)	6.7	7	7
Rising / falling times (ps)	74	$t_r = 64$ $t_f = 56$	$t_r = 68$ $t_f = 62$
Propagation delays (ps)	151	$\tau_{PHL} = 158$ $\tau_{PLH} = 156$	$\tau_{PHL} = 182$ $\tau_{PLH} = 180$
Power consumption (mW)	9.2	10	9.9
Energy efficiency (pJ/bit)	1.4	1.5	1.4

This can explain discrepancy observed in particular for power consumption.

V. Conclusions

In this paper, the optimization of a silicon photonic transmitter is demonstrated based on a Mach-Zehnder interferometer and an asymmetric driver implemented in a CMOS 0.18 µm technology. The logical effort method is employed to size both *Driver Anode* and *Driver Cathode*. The trade-off between data rate, power consumption and circuit area is explored via slew-rate limitation, in order to be able to adapt the driver design to specifications. Good agreement is shown between early-design-stage equations and post-layout simulation results. Therefore, such optimization technics can continue to be used to boost data rates with shrunk CMOS nodes and improved electro-optic modulators.

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