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***Abstract*—The demand for high resolution CMOS image sensors (CIS) is rising. Analog-to-digital converters (ADC) represent one of the major bottleneck of CIS. One of the candidates to overcome the existing limits is the column-parallel ADC. Column-parallel extended counting ADCs (EC-ADC) are able to reach high resolution thanks to their two-step conversion. However the EC-ADC area increases due to the two-step design. A solution is to use the same hardware twice to perform both steps. This paper proposes a 14-b, 100 kHz Nyquist frequency, two-step incremental ΣΔ (IΣΔ) analog-to-digital converter suitable for column-parallel CIS. Several architectures with different modulator order are compared to determine the most promising one. The proposed architecture, compared to a one-step second order modulator, reduces the total oversampling ratio (OSR) from 150 to 60 to reach a resolution of 14-b. The operational transconductance amplifiers (OTA) is the most critical part in our ADCs. Its required DC-gain is around 80 dB for a 120 MHz gain-bandwidth product (GBW). The ideal DNL and INL of our two-step IΣΔ ADC are respectively +0.55/-0.6 LSB and +0.5/-0.5 LSB. This work achieves a SNDR of 89 dB when a full scale sinusoid of 100 kHz is applied.**

***Index Terms*—ADC, incremental, sigma-delta (ΣΔ), two-step, CMOS Image Sensor, column-parallel ADC, second-order ΣΔ**

I. Introduction

High quality CMOS image sensors (CIS) have become indispensable in the aerospace field. This evolution is possible thanks to the progress in the integration of sensor, readout electronics and A/D conversion in a single chip. The increasing resolution of the image sensor restricts the pitch of the pixel. This also increases the rate of pixel data conversion for a given frame rate. Moreover, greater pixel sensitivity and dynamic range demand 12-bits or higher resolution conversion. The column-parallel conversion is seen as the best answer to these increasingly stringent requirements.

Among column-parallel ADCs, single-slope (SS-ADC) and successive approximation register (SAR) ADCs are usually chosen for low power consumption application [1] [2] [3] [4]. However, the SS-ADC requires a large amount of clock cycles for high resolution conversion. The SAR ADC needs a capacitor DAC consuming large area due to the weight of the capacitor and is very sensitive to the capacitor mismatch. Cyclic ADCs are also widely used in the CIS field [5] [6] [7]. This ADC only requires n clock cycles for a n-bit resolution. However, cyclic ADCs require high DC gain OTA to avoid non-linearity. Matching problems limit the resolution achievable by cyclic ADCs. Sigma-Delta (ΣΔ) ADCs are well known for their ability to achieve high resolution. However they are slower than Nyquist converters due to oversampling. ΣΔ ADCs have recently appeared in CIS field thanks to the scaling down technology [8] [9]. ΣΔ ADCs require smaller DC gain and sampling capacitance than cyclic ADCs because of the oversampling operation.

In order to achieve a better tradeoff between speed and resolution, extended-counting ADCs (EC-ADC) have been reported [10] [11]. The EC-ADC is an hybrid architecture that performs the conversion in two steps. First a coarse conversion is done using an incremental ΣΔ (IΣΔ) ADC. The first step generates an analog residue. Then the fine conversion of the residue is realized with a Nyquist converter. Thus the overall conversion time is reduced compared to a single step IΣΔ. However EC-ADCs have quite complex circuits due to the use of two different conversion principles. The two-step conversion can be pushed further and both conversions can be realized by the same IΣΔ ADC. Such architectures are known as two-step IΣΔ ADCs [12] [13]. The two-step IΣΔ ADCs advantage is to use twice the same hardware for both conversions, while simultaneously decreasing the overall OSR. In order to obtain a higher resolution (compared to a single loop IΣΔ) and limit the complexity of the circuit, a two-step IΣΔ ADCs can be preferable over EC-ADCs. In this paper, a two-step second order IΣΔ ADC is proposed. The remainder of this paper is organized as follows : section II describes the IΣΔ modulator. In section III a two-step IΣΔ architecture and its characteristics are described. In section IV the high level modulator design is discussed. Then the section V presents

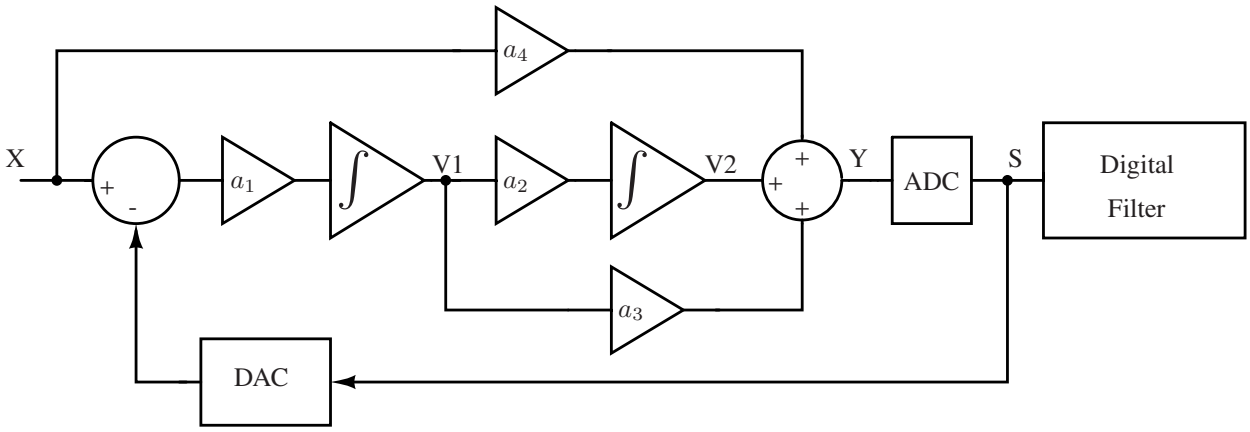


Figure 1. 2^{nd} order modulator with feed-forward path

the simulated ADC characteristics.

II. INCREMENTAL ΣΔ ADC

The first IΣΔ ADC was published by Van De Plassche in 1978 [14]. It is composed of an integrator, an ADC (a comparator with 2 levels in most cases) and a digital-to-analog converter (DAC) in the feedback path. This architecture has the drawback to be very slow. Indeed it requires 2^n clock cycles to reach *n*-bits. To improve the conversion speed, one can increase the modulator order or the number of cascaded modulators. However, higher order modulators can lead to stability problems which are hard to solve. An example of a IΣΔ with a second order modulator is shown in fig.1. Here, the IΣΔ is studied in the time domain. In this way the residue value can be written depending on ΣΔ modulator parameters and the result is reused later for the two-step architecture. In this architecture the output of the integrators are given by

$$V_1[M] = a_1 \sum_{i=1}^{M-1} (X[i] - S[i]) \tag{1}$$

$$V_2[M] = a_1 a_2 \sum_{K=1}^{M-1} \sum_{i=1}^{K-1} (X[i] - S[i]) \tag{2}$$

where *M* is the OSR. After *M* clock cycles the error of conversion is given by

$$E \;=\; X - \hat{X} = \frac{2}{a_1 a_2 M(M-1)}.V_2[M] \tag{3}$$

where $\hat{X}$ is the estimated reconstructed signal from the bitstream, defined as,

$$\hat{X} = \frac{2}{M(M-1)} \sum_{K=1}^{M-1} \sum_{i=1}^{K-1} S[i] \tag{4}$$

One can observe that the residue value $V_2(M)$ is the image of the conversion error. With this modulator, 150 cycles are needed to reach 14 bits resolution [15].

III. TWO-STEPS IΣΔ ADC

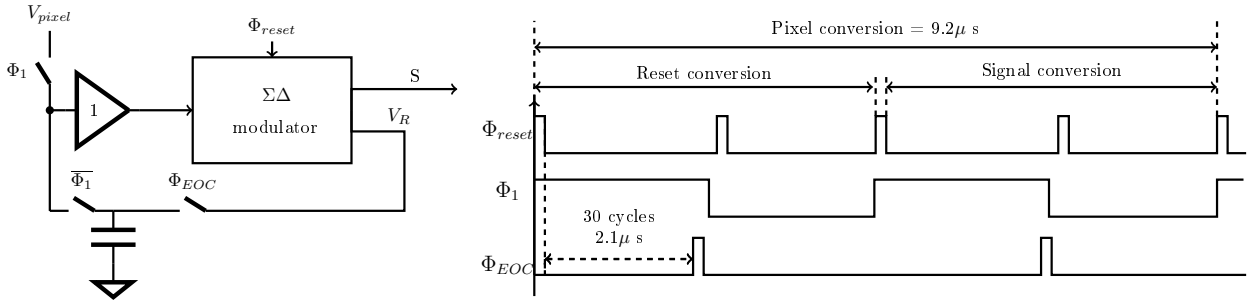
A. Two-steps architecture

For several years, architectures with reused hardware have been investigated to decrease the size of the ADC [16] [17] . In a two-step IΣΔ ADC [12] [18], the conversion is divided in 2 phases and the hardware is used twice to perform the full conversion. The chosen architecture and its diagram timing are shown in fig.2.

The architecture is composed of a sample-and-hold (S/H), an IΣΔ modulator and a digital filter. At the beginning of the conversion, a reset is done on the integrators and the capacitors. During the first step (Φ1=1) the pixel value is fed to the modulator. At the end of the coarse conversion ($\Phi_{EOC} = 1$ and Φ1=0), the residue V_R (or V_2[M]) is loaded into the S/H. Then another reset is done and the fine conversion is performed. The timing diagram for a conversion is shown in fig. 2(b). To reach 100 frames/s (FPS) with a 1920x1080 array, the available row time is 9.2 μs. Two conversions are realized within the row time to do a correlated double sampling in digital domain. Since a few extra clock cycle are necessary to reorganize the switch and load the capacitance, a single step can last up to 2.1 μs.

B. Modulator scaling

As already mentioned the residue of the coarse conversion is used for the fine conversion. The goal is to fit the output of the first step to the input of the second step. Moreover the input range of a 2^{nd} order modulator must be limited to avoid integrator overflow. So it is very important to limit the residue value. The chosen modulator is shown in fig.1. As one can see in eq.(3), a solution to modify V_R is to modify the parameter $a_{1,2}$ of the modulator. In fig.1, parameters a_1 and a_2 are arbitrary chosen at 0.5 and the maximum input at 75% of the reference. An optimization is performed by sweeping parameters a_3 and a_4 to minimize the swing of the signals into the integrators giving a_3 = 2 and a_4 = 1. Then a global scaling coefficient is applied to fit the output swing



(a) (b)

Figure 2. High-level view of (a) two-steps architecture with 2^{nd} order modulator and (b) the timing diagram of the conversion

of the integrator with the input range of the modulator. The optimum coefficients are a_1 = 0.75, a_2 = 0.5, a_4 = 1.5 and a_3 = 2. However these optimal values are not very convenient to implement in switched capacitor circuit. Moreover a margin has to be taken from optimal coefficients to be insensitive to analog mismatches. At the end, the final values are a_1 = a_2 = 0.5, b_1 = 1 and a_3 = 2.

From eq.(3) a total of 27 cycles per step is needed to reach 7-b of resolution. In order to get some margin to deal with analog mismatches, the OSR is increased to 30 leading to a total OSR of 60 for a conversion giving 70 ns per cycle. Once again, a small margin is taken giving a clock frequency of 20 MHz.

C. OSR split of two-steps conversion

We previously supposed that the length of both steps were equal. This supposition is verified in the following part as the optimal choice. The parameters $k1 = a_1.a_2.M_1(M_1-1)/2$ and $k2 = a_1.a_2.M_2(M_2-1)/2$ are introduced with M_1 and M_2 respectively the OSR of the first and the second step. From eq.(3), one can derive the error of the conversion,

$$E_{TOT} = \frac{V_{FS}}{k1.k2} = \frac{4}{a_1^2.a_2^2.M_1(M_1-1).M_2(M_2-1)}.V_{FS}$$

$$E_{TOT} \approx \frac{4}{a_1^2.a_2^2.M_1^2.M_2^2}.V_{FS} \quad (5)$$

Setting $M = M_1 + M_2$ and $\alpha = M_1/M_2$, eq.(5) can be written,

$$E \approx \frac{4.V_{FS}}{\frac{a_1^2 a_2^2 \alpha^2.M^4}{(\alpha+1)^4}} \quad (6)$$

From eq.(6), one can plot the curve shown in fig. 3. As one can see the resolution is maximum when the OSR is equal in both steps.

The choice of the modulator order for the two steps is now discussed. In recent two-step IΣΔ ADC work, the modulator order can be different for the two-step [18]. For second and higher order modulator, the last integrator can be switched to a sample-and-hold for the second step. The modulator order of the second step is then decreased of one order. The analysis of the modulator order within the conversion is now studied. Four different architectures are compared : a third order modulator single loop (IΣΔ3), a two-step with a second and first order modulator (IΣΔ2-1), a two-step with two second order modulator (IΣΔ2-2) and a two-step with a third order and second order modulator (IΣΔ3-2). The result of our simulations is shown in fig.4. The resolution of the different ADC is calculated from the conversion error, computed using eq.(5). In each case, integrators modulators coefficients and α in eq.(6) are optimized to minimize the conversion error, thus maximize the resolution. In the different architectures, input range is reduced to avoid integrator overflow. Considering the scaling of the different architectures and the aimed resolution, the proposed IΣΔ2-2 architecture requires the smallest OSR.

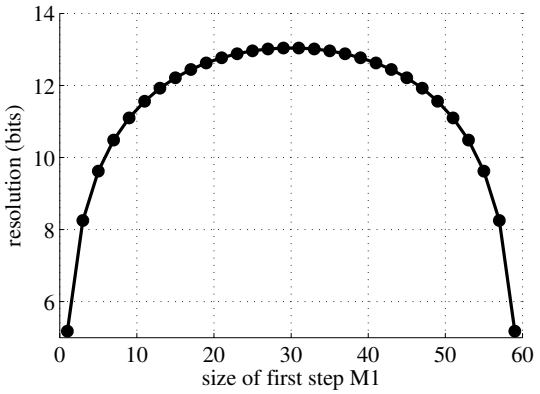


Figure 3. resolution of the conversion for different size of the first conversion

IV. Modulator specifications

In this section, the switched capacitor circuit and the modulator characteristics are presented. The effect of non-idealities in the OTA (finite DC gain, gain bandwidth-product (GBW) and slew rate (SR)) are introduced and their effects simulated. In this part and for the rest of the paper, the resolution is calculated from the SNDR.

A. Switched-capacitor circuit

The switched-capacitor circuit implementation is shown in fig. 5. A single-ended version of the architecture is represented to simplify the circuit. The sampling capacitance

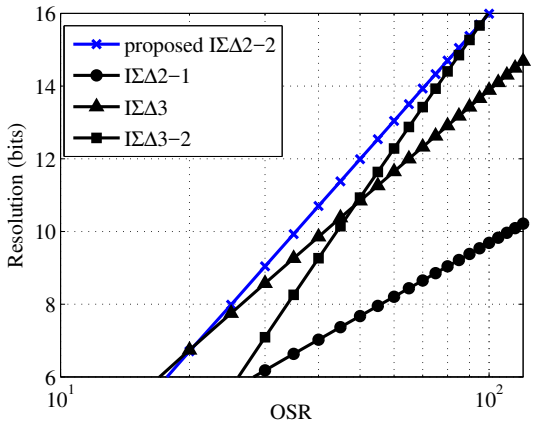


Figure 4. comparison of different architectures and modulator order

C_s is chosen to be 100 fF. The integrators realized with the OTA are the most critical part in a modulator. To minimize injection charge effect, two non overlapped clock p1 and p2, and their delayed signal p1d and p2d, are used

The characteristics of the OTA are now discussed. The DC gain OTA, the GBW and the slew-rate (SR) are important parameters in a switched capacitor circuit. These parameters are degrading the charge transfer and introduced errors at both input and output of the integrator.

B. Finite OTA DC gain

The finite DC gain OTA introduces an offset at the input of the integrators. The transfer function of the integrator with an finite OTA DC gain is expressed as follow

$$Vo(n) = \frac{(1+\mu)Vo(n-1) + \frac{C_s}{C_i}Vin(n-1)}{1+\mu(1+\frac{C_s}{C_i})} \quad (7)$$

with Vo the output of the integrator, Vin the input, $\mu = 1/Ao$, with Ao the finite DC gain, C_s and C_i respectively the sampling and the integrator capacitance. The simulation is shown in fig.6. One can see that the resolution drops from a DC gain of 5000, or 74 dB. Thus a minimum DC gain of 80 dB is chosen.

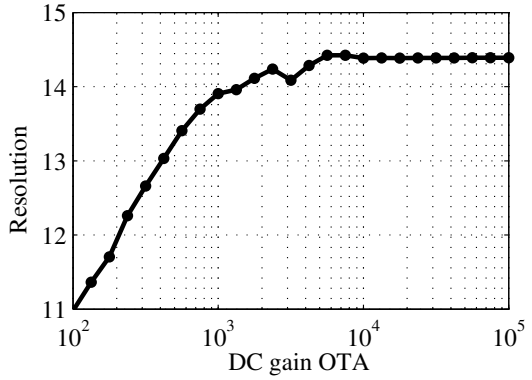


Figure 6. DC gain OTA versus ENOB

C. Finite GBW and SR

The charge transferring phase of a switched-capacitor circuit can be cut into a slewing and a settling part. Finite SR and GBW respectively influence the slewing and the settling time. The influence of the GBW on the system is first analysed. The transfer function of an integrator with a finite GBW is

$$Vo(n) = Vo(n-1) + \frac{C_s}{C_i}\left(1 - \exp^{-k_1}\left(\frac{C_s}{C_s+C_i}\right)\right) \quad (8)$$

with

$$k1 = \left(\frac{GBW.C_i}{C_i+C_s}\right)\left(\frac{T}{2}\right) \quad (9)$$

with Vo and the Vin respectively the output and the input of the integrator and T the available settling time. The result of the simulation is shown in fig 7. One can see that the

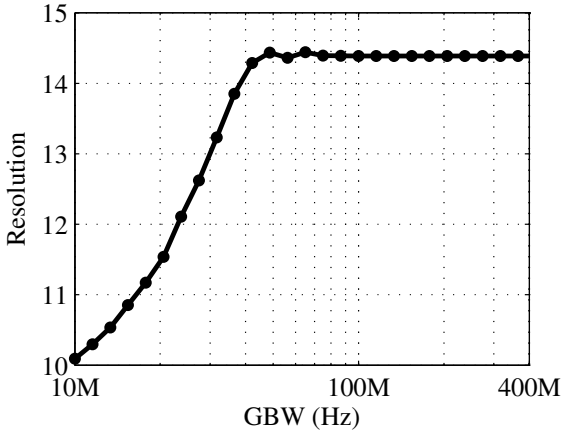


Figure 7. DC gain OTA versus ENOB

resolution quickly dropped for a GBW below 50 MHz. However this value is quite small considering the settling time. Thus a GBW of 120 MHz is chosen to be at least five times higher than the clock frequency. The slewing time is then determined to calculate the SR. A good trade-off is to set the slewing time at 25% of the available time. The remaining time is used for the settling time. The SR is expressed by

$$SR = \frac{\Delta V}{T_{slewing}} \quad (10)$$

with ΔV the maximum output swing of the integrator and $T_{slewing}$ the chosen slewing time. The minimum SR calculated is 220 V/μs. The values found previously are put together in table I.

V. Results

An ideal model of the proposed ADC is used to compute the DNL and the INL of the ADC. The ideal DNL and the INL of the IΣΔ are shown in fig.8 and fig.9. The DNL and INL of the ADC are respectively +0.55/-0.6 LSB and +0.5/-0.5 LSB. The ADC output spectrum is shown in fig.10. The SNDR is calculated with a full scale input signal of 100 kHz

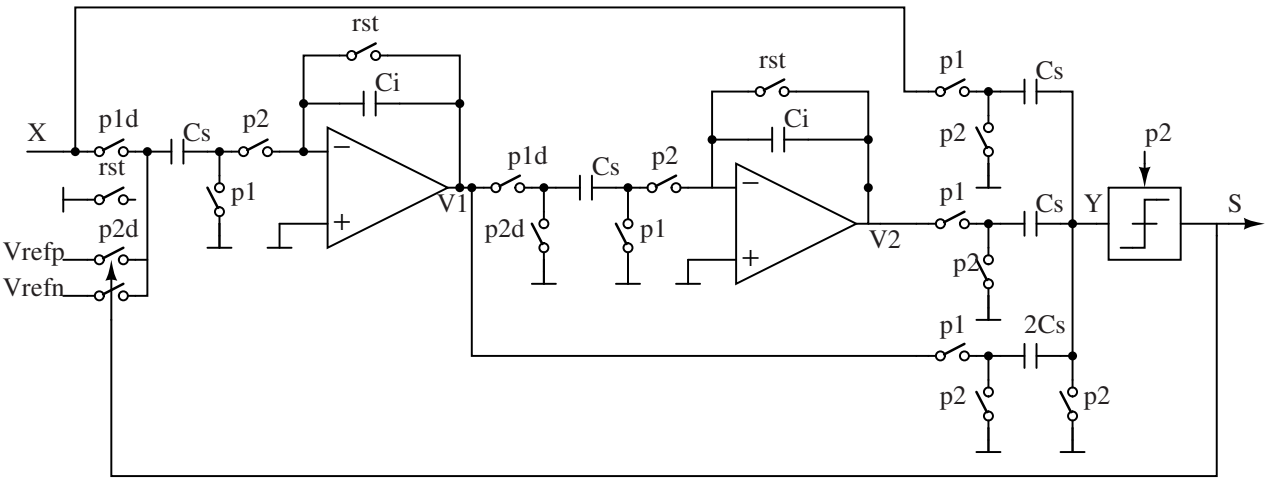


Figure 5. 2^{nd} order modulator with feed-forward path

Table I
OTA CHARACTERISTICS

Slew rate	220 V/μs
GBW	120 MHz
Load capacitance	300 fF
DC gain	80 dB

and a sampling frequency of 20 MHz. This ADC achieves a SNDR of 89 dB. The power consumption is estimated from schematic simulation and is 450μW. The performance comparison with others EC-ADC is shown in table II.

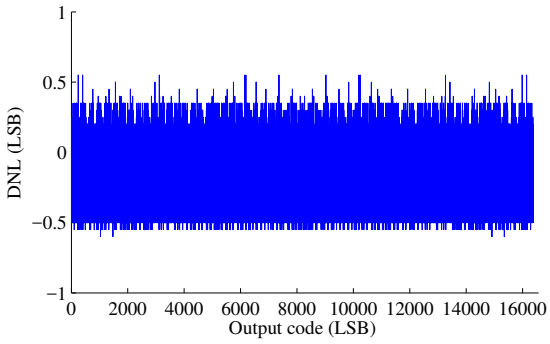


Figure 8. DNL of proposed ADC

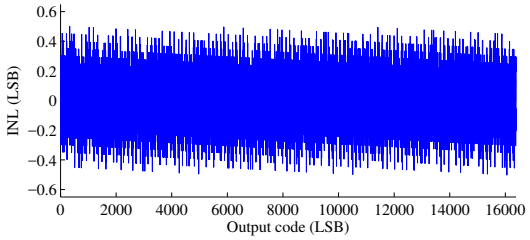


Figure 9. INL of proposed ADC

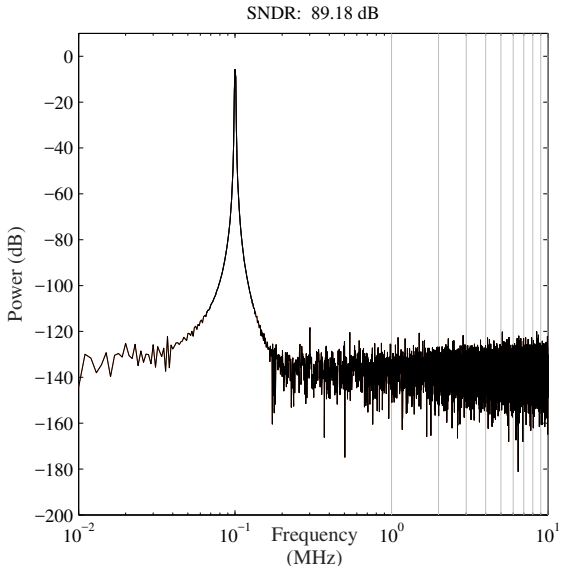


Figure 10. ADC output spectrum

VI. CONCLUSION

This paper presents a two-step IΣΔ for column-parallel conversion of pixel arrays, allowing a monolithic integration of the whole CIS. First, several architectures are compared to analyze the one reaching the highest resolution with the lowest OSR. Compared to a single loop second order modulator, the proposed two-step ADC with second order modulator (IΣΔ2-2) can reduce the OSR from 150 to 60, to reach 14-b of resolution. Simulations are then realized to get OTA specifications that avoid lowering the resolution of the ADC. To finish simulations on ideal (IΣΔ2-2) ADC

Table II
PERFORMANCE COMPARISION

	[11]	[19]	[10]	[12]	This work
Technology (μm)	0.18	0.35	0.18	0.15	0.18
ADC architecture	$\Sigma\Delta$+Cyclic	$\Sigma\Delta$+SAR	$\Sigma\Delta$+Cyclic	2step $\Sigma\Delta$	2step $\Sigma\Delta$
Sampling rate (kS/s)	30	150	50	-	100
Resolution	17	14.3	10.2	12	14
Power (μW)	345	300	13	363	410
DNL (LSB)	-0.88/1.38	-0.79/0.97	-	-0.7/1.8	-0.55/0.6
INL (LSB)	-26.3/35	-1.7/2.79	-	-22/20	-0.5/0.5
SNDR (dB)	85	-	63	-	89

are performed giving DNL/INL characteristics and the ADC output spectrum.

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