

Monolithic integration of mutually injection-locked CMOS-MEMS oscillators for differential resonant sensing applications

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Abstract— Differential architectures based on two injection-locked MEMS oscillators are a promising technique for high-end resonant sensing applications since they enable environmental drift rejection and high sensitivity. But properly coupling two M/NEMS resonators together is challenging. In order to eliminate drift, the resonators must be fabricated very close to each other and to be as well-matched as possible. To this end, both resonators and the circuitry can be monolithically-integrated on a single chip. However this leads to parasitic coupling and feedthrough, which affect the performances. This paper explains how, block by block, our architecture and our chip are designed to minimize these spurious couplings. The improvements resulting from the optimization of the ASIC are illustrated by simulated and experimental results.

Keywords—CMOS-MEMS; MEMS resonators; injection-locked oscillators; resonant sensors

I. INTRODUCTION

The main challenge when designing a good sensor is maximizing the sensitivity to the quantity of interest while minimizing its sensitivity to every other parameter (environmental drifts). As MEMS resonators emerged as good candidates [1] for high-end applications and embedded systems due to their low foot-print, low electrical consumption and possibly very high sensitivity, their sensitivity to external drifts (especially temperature and pressure) rapidly became an issue.

Several techniques were developed, mainly using active compensation of the environmental drifts, like micro-ovens [2] and encapsulated atmospheres. But as the micro-oven is already power- and area-consuming, they rely on a precise temperature sensor and dedicated electronics for the control which increases the footprint even more [3]. Using a second MEMS resonator with different temperature dependence was proposed as a solution for temperature sensing but putting both resonators close to each other was necessary in order to ensure that they both were undergoing the same temperature variation. Parasitic coupling leading to frequency pulling and locking was thus inevitable [4]. Recently the idea of using two different bulk modes of a single MEMS resonator, with very different

natural frequencies was proposed, but it requires extensive electronics [5].

Our proposition is to enforce two similar resonators into a synchronized (injection-locked) state through their actuation voltages. In theory, this makes it possible to overcome weak, spurious couplings and to achieve high-sensitivity differential (i.e. drift free) measurements. Furthermore, the proposed architecture does not require any complex electronics and is entirely VLSI. In our previous work [6] [7], the MEMS resonators are fabricated separately, and thus suffer from mismatches resulting from variations in their fabrication process, and they are mounted on different PCBs, so that they are not subject to exactly the same environmental drifts. In the present work, we present a new fully co-integrated chip, where the resonators are fabricated as close to each other as possible, in order to (i) optimize the errors due to the fabrication process and reduce the inherent mismatch and (ii) make sure they undergo the same environmental drifts.

This paper focuses on the circuit design, from the co-integration of CMOS-MEMS resonators to the complete differential architecture. In section II the concept of strong coupling for differential sensing is quickly described. In section III we address the design of the blocks and how they are put together on a single chip. Some simulated results of the expected differential sensitivity and drift rejection are given and commented on section IV. Simulations are carried out using Virtuoso Spectre. RLC models of the MEMS resonators are employed since they operate in the linear zone (see [8] Appendix A for the calculation).

II. MUTUALLY INJECTION-LOCKED OSCILLATOR (MILO)

A system-level description of a MEMS-based MILO is represented in fig. 1. It is composed of three parts: the two CMOS-MEMS resonators and a mixer enforcing strong coupling and the self-oscillation of the loop. Nominally, the resonators are supposed to have the same quality factor Q , and natural frequency. The mixer ensures a strong, highly non-linear coupling maintaining both resonators in a synchronized oscillation state. Proper modeling and theoretical results are presented in [8], covering several possibilities for the implementation of the mixer's architecture. Typical waveforms (analog front-end outputs and excitation voltages) are represented fig. 2. The phase difference between the resonator's outputs V_1 and V_2 (or equivalently the duty cycle of

V_{f1} and V_{f2}) can then be monitored to track changes in the system parameters:

- when the natural frequencies of the resonators are subject to the same variation (e.g. through temperature drift or other “common-mode” variation), the phase difference remains unchanged whereas the frequency of the MILO changes adequately.
- when the natural frequencies of the MEMS resonators are subject to differential variations, the phase difference changes as a result. The relative phase difference variation is on the order of Q times more important than the relative oscillation frequency variation.
- the phase difference is relatively insensitive to variations of other parameters of the system such as amplifier gain, phase delay in the blocks, quality factor, etc. This makes the device robust to process variability.

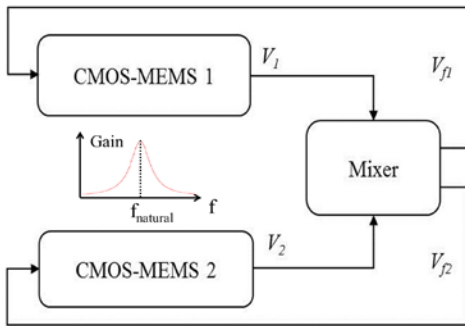


Figure 1. System-level description of a MEMS-based MILO, and typical frequency response of CMOS-MEMS resonator.

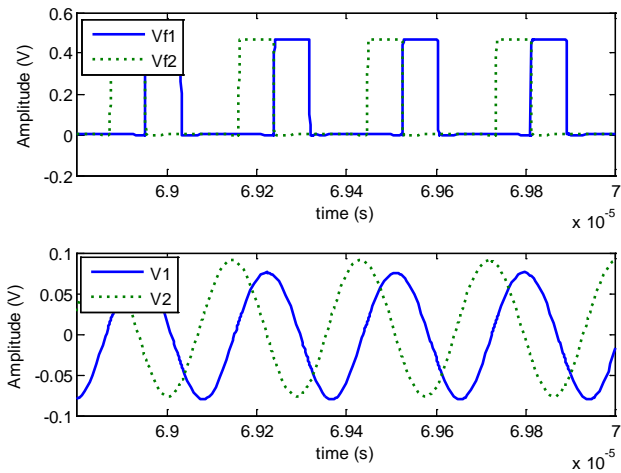


Figure 2. Simulated waveforms of the MILO

Thus, monitoring the phase difference theoretically enables a highly sensitive, drift-free measurement of a physical quantity. But this requires very similar MEMS resonators, as close to each other as possible. A first experimental proof of

concept of the properties of this sensor architecture, based on a discrete implementation of the architecture of Fig. 1, is given in [7]. In section III, we address the issues raised by the monolithic integration of the architecture.

III. CHIP DESIGN AND CO-INTEGRATION

The MILO presented in fig. 1 is now transistor-level designed and co-integrated on a single chip. Based on previous implementation results [7], a digital mixer and output buffer are designed. In order to obtain on-chip signals similar to presented in fig. 2, the output buffer should be able to drive 20 pF of PADs and probe connections. We also design decoupling capacitances to avoid spurious coupling through the power supply. This section provides details about every components of the co-integrated MILO.

A. CMOS-MEMS resonators

Each CMOS-MEMS resonator actually consists of one amplifier and two MEMS beams. The beams are tungsten cantilevers with dimensions 10 μm length, 500 nm width, 900 nm thickness and electrostatic actuation and detection gaps of 450 nm. Such structures have a natural frequency around 3.3 MHz and a quality factor around 170 in air. The differential amplifier used in this work was previously presented in [9]. A resonator is connected to each input of the amplifier differential pair, but only the one on the non-inverting input is biased (the “active” MEMS), whereas the other (the “dummy” MEMS) is not biased. This makes it possible to amplify the motional current of the biased resonator, while canceling out the parasitic current caused by capacitive feedthrough. The fig. 3 presents a schematic of a differential CMOS-MEMS structure, and a scanning electron microscope (SEM) image of the active and dummy MEMS beams.

The signal is then buffered in order to be able to deliver enough output current to drive the mixer and the scope. Fig. 4 presents the open-loop responses of two separately-fabricated CMOS-MEMS resonators [7]. The absence of anti-resonance demonstrates the efficient feedthrough cancellation. The difference in the gain- and phase- response of the chips is due to variations in their fabrication process (different etching times). These issues can be avoided by integrating the resonators in a single chip.

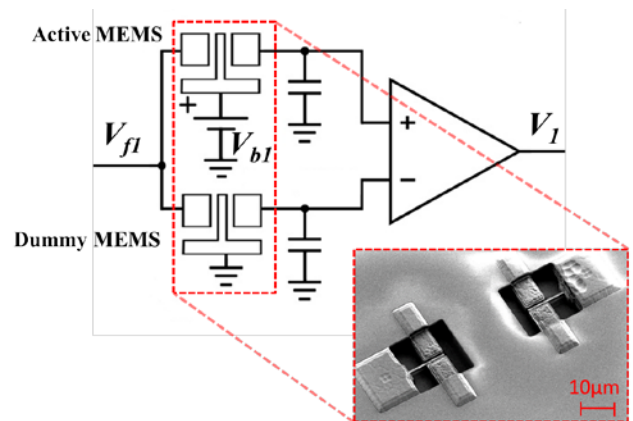


Figure 3. Schematic of a differential CMOS-MEMS resonator and SEM view of one pair of active and dummy cantilever beams (with a 35° tilt).

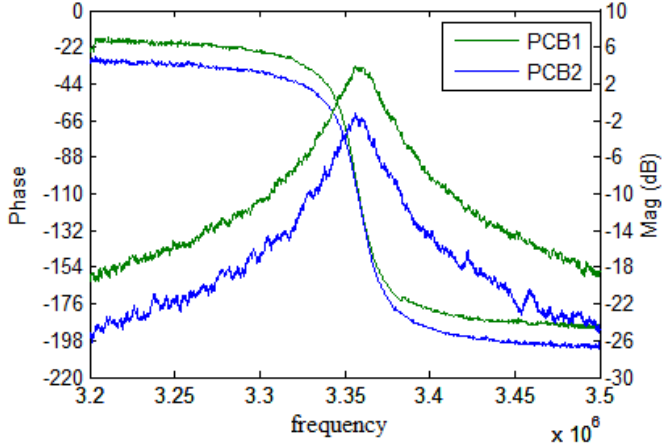


Figure 4. Frequency responses of two separately-fabricated CMOS-MEMS resonators.

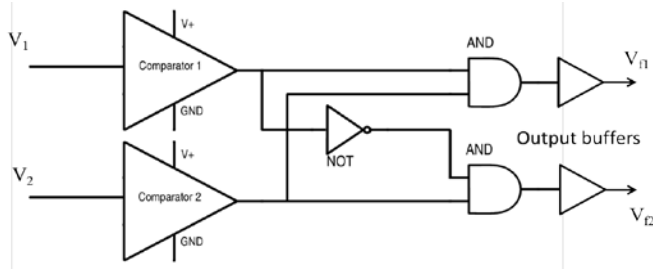


Figure 5. Schematics of the digital mixer and the output buffers

B. Digital mixer

The digital mixer is composed of two comparators, two AND gates and one NOT gate as shown fig. 5.

Comparators are found in AMS 0.35um A_CELLS library. They provide a 17 mV hysteresis on the negative threshold which disables unwanted trigger. Their rise and fall time is 7 ns. The digital gates are chosen with minimal fan-out to minimize the parasitic capacitances in the feedback nodes. They are found in AMS 0.35um Digital Cell library.

C. Output buffer

Since the digital mixer's topology is designed using minimal gates, output buffers are required to drive the PADs and the scope. The output capacitance to load is estimated at 20 pF. We implement an optimization between the output resistance, and thus the rising time of V_{f1} and V_{f2} , and the propagation delay in the buffers. To this end, a 4-stage of increasingly larger inverter gates is designed. The inverter gates are also found in the AMS Digital library.

D. Decoupling capacitances

The digital mixer and buffer induce important current spikes, from which the analog part of the system must be screened in order to preserve the frequency stability of the MILO. To solve this issue, a matrix of decoupling capacitors is added. The unitary decoupling capacitor is a $10 \times 10 \mu\text{m}$ NMOS transistor in the inversion region towered by an interposition of metal layers. This association produces a 50 fF capacitor with low access resistance.

Power supply and ground are routed through this matrix, providing a very low-resistive and decoupled 3.3 V, reducing power-supply drops due to the current spikes of the digital part. The equivalent decoupling capacitor is 40 pF; and it is distributed in the chip by a capacitor matrix.

IV. SIMULATION RESULTS

The co-integrated MILO is designed using AMS 0.35 technology, consuming an area of $2.4 \times 0.175 \text{ mm}$. Post-layout simulations are performed with Virtuoso Spectre. These simulations are compared to the experimental results obtained with (i) the discrete implementation of the system [7], and with (ii) a fully-integrated MILO, without output buffers or decoupling capacitances.

A. Effects of design on the steady-state behaviour

We simulate the steady-state of our device and compare it to our previous work. We consider in particular the effect of the buffer on the actuation waveforms.

The output of the mixer-buffer can be considered as a RC filter, with R the output resistance, and C the capacitance to load. The first device (i) is made of discrete components and requires a lot of wiring between the blocks. The capacitance to load is high, around 285 pF, and even though the integrated circuits have buffered outputs, the rise and fall time are 40 ns. The second device (ii) is fully co-integrated but with no output buffer, thus the output resistance is high at 1.1 k Ω . Even though the capacitances to load are much smaller, around 20pF, the rise and fall time are 66 ns. The device presented in section III is co-integrated and has an output buffer. The simulated load capacitance is 20 pF. The output resistance is 82.5 Ohms. Thus the rise and the fall time are 5 ns. Results are summarized in table I. The signals obtained with a transient post-layout simulation of the new device are compared to experimental measurements of the previous co-integrated device (ii) in fig. 6. This validates the output load requirements.

Transient simulations of the different co-integrated devices (with and without buffer) are made and presented fig. 6, illustrating the effect of the buffer on the rise and fall time.

Table I: Effect of the buffer and co-integration on the rise and fall time of the digital mixer.

	discrete device [7]	Co-integrated w/o output buffers device	This work
Rise time	40ns	66ns	5ns

B. Effects of design on the device's performances

We first simulate an environmental drift of the chip, in order to test the common mode rejection of our architecture. We then simulate an electrostatic stiffness mismatch in order to assess its sensitivity.

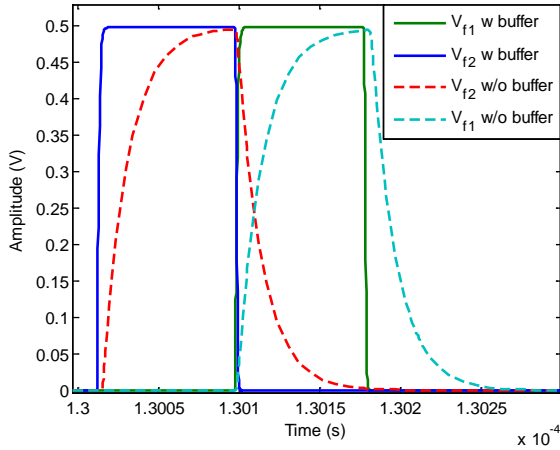


Figure 6. Comparison of actuation signals with and without output buffers.

The change of temperature of the chip has two effects. First, the Young's modulus of tungsten changes according to [10]. RLC models are calculated to include this change. Then, the performance of the circuitry change as well, which is taken into account by the simulator. The chosen temperature range is from $-20\text{ }^{\circ}\text{C}$ to $80\text{ }^{\circ}\text{C}$. We then perform the same kind of simulation, but this time changing the bias voltage of one of the resonators from 29.5 V to 30.5 V , leaving the other one at 30 V , and at room temperature ($20\text{ }^{\circ}\text{C}$). Due to the electrostatic stiffness change, this results in a mismatch of the natural frequencies of the resonators. Temperature- and voltage-sensitivity coefficients of the oscillation frequency and of the phase difference can then be calculated to derive a model of the sensor:

$$\begin{cases} f = 3.29 \cdot 10^6 \cdot \left(1 + \alpha \cdot \frac{\Delta V}{V_b} + \gamma \cdot \frac{\Delta T}{T_{amb}}\right) \\ \varphi = \frac{\pi}{2} \left(1 + \beta \cdot \frac{\Delta V}{V_b}\right) + \delta(T) \end{cases} \quad (1)$$

where ΔT is the temperature change, ΔV the biasing voltage mismatch, φ the phase difference between the resonators and f the frequency of the MILO. The parameters α and β are the relative frequency and phase difference change due to a biasing voltage mismatch. γ is the MILO's frequency change with the temperature of the chip. It is mostly impacted by the change of Tungsten's Young's modulus with temperature, but also the change of behavior of the CMOS components. Finally δ is the sensibility of the phase difference to the global change of temperature of the chip. The extracted values of these parameters are reported in table II. In both cases, the ratio of α and β agrees very well with the theory [8].

Table II: Simulation results of the common mode rejection and sensitivity to mismatch of the MILO

	α	β	γ	δ
This work (simulations)	$15 \cdot 10^{-3}$	9.77	$1.5 \cdot 10^{-3}$	$\pm 0.25^{\circ}$ [-20°C, 80°C]
Previous work [7]	$14.1 \cdot 10^{-3}$	9.87	$1.6 \cdot 10^{-3}$	$\pm 1^{\circ}$ [25°C, 65°C]

One main results stands out from these simulations: compared to [7], the stability of the phase difference with the temperature (or drift-rejection) of the device is enhanced by 4. Note that the temperature range used in the simulations is about three times larger than the one that was experimentally achieved.

V. CONCLUSION

In this paper we presented the design of a fully-integrated MEMS-based MILO. As shown by post-layout simulations, reducing the fabrication mismatch between the resonators enables a much better drift rejection, since we obtain an 4 times more stable architecture over a much larger temperature range. We also showed how a careful design could notably improve the actuation waveforms of the resonators, and reduce spurious couplings between them. Our ongoing work will now be to make experimental measurements of the fully-integrated chip as soon as it is fabricated. We will then focus on the development of a closed-loop controller to extend the locking range of the architecture by electrostatic stiffness tuning.

This work has been partially financed under project number TEC2015-66337-R (MINECO/FEDER)

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