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***Abstract*—This paper presents envelope elimination and restoration (EER) architecture specifications in the case of orthogonal frequency division multiplex C band transmission. A key point is the recombination of envelope and phase information by supply modulation of the power amplifier (PA). Imperfections, such as time mismatch and phase noise can reduce the performances of the transmission. Compression and conversion effects when supply modulating the PA are introduced in this paper with the simulation of a class E power amplifier. This amplifier was designed under HP-ADS using a nonlinear Mesfet model. Results are reported in terms of error vector measurement and spectrum for two different numbers of sub-carriers 32 and 128 in 16-QAM and 64-QAM cases.**

***Index Terms*—Class E, envelope elimination and restoration (EER), orthogonal frequency division multiplex (OFDM).**

I. Introduction

An ENVELOPE elimination and restoration (EER) architecture [1] is based on the decomposition of the emitted signal in envelope and phase parts. In the case of an orthogonal frequency division multiplex (OFDM) signal, the envelope is highly variable (Peak to Average Power Ratio is majored by N, where N is the number of sub-carriers). After amplification, the recombination of the envelope and phase information is accomplished by drain modulation of an amplifier such as class E type as illustrated in Fig. 1 [2].

In order to give specification for C band OFDM transmitter (802.11a or Hiperlan2), we introduced imperfections on HP-ADS simulations. Previous works in [4] and [3] demonstrated the impact of time mismatch, IQ modulator default and phase noise. A cosimulation of a class E amplifier, with $\mathrm{V_{dd}/AM}$ and $\mathrm{V_{dd}/PM}$ nonlinear response, is realized here. Results are given in terms of spectrum and error vector measurement (EVM) [according to IEEE 802.11a standard formula]. Different schemes are simulated by varying the number of sub-carriers (32 or 128) and using a 16 or a 64-QAM. The symbol frequency is set to 20 MHz.

II. Results From Previous Works

In [4] was specified the influence of time mismatch, IQ impairments and phase noise. Results showed the importance of the signal dynamic on EER architecture. The higher the number of sub-carriers, the higher the EVM. Time delay is a critical point [3]. A synchronization method has to be used to reduce the mismatch under 5% of the symbol time. This imperfection causes no more than 2.5% of EVM. The phase noise of the synthesizer profile has to be kept as low as −95 dBc/Hz at 100 kHz from the carrier. Finally, IQ modulator will have to be tuned. Typically −40 dB for image rejection ratio (IRR) and −36 dB for oscillator rejection (OLR) have to be achieved. These two imperfections debase EVM to approximately 4.6%. The emitted spectrum suffers from spectral regrowth as illustrated in Fig. 2.

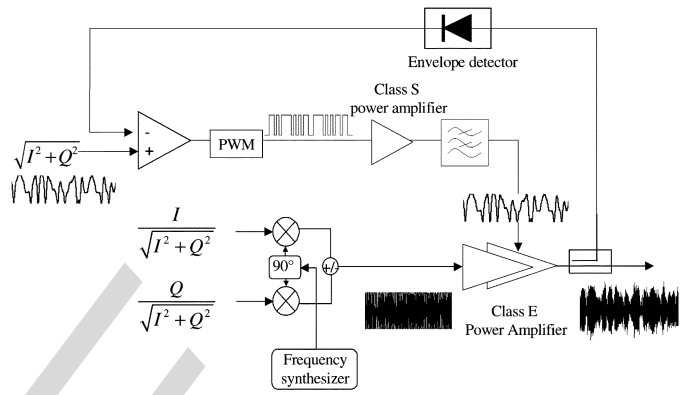

Fig. 1. EER architecture principle.

Firstly $\mathrm{V_{dd}/AM}$ and $\mathrm{V_{dd}/PM}$ compression and conversion effect due to supply modulation [4] were simulated with a polynomial approximation. Results pointed the need of linearization, especially for conversion effect as demonstrated in Table I. Secondly a real class E amplifier was designed in this paper to refine these results, obtained using HP-ADS envelope simulator (see Table II).

III. Class E Amplifier

Class E amplifier theory is introduced in [5] and [6] where reactance values of the loading network are mathematically demonstrated. Theoretically this amplifier has an efficiency of 100%. This efficiency can only be achieved with an infinite quality factor for the filtering part, with a zero saturation resistance and with a perfect switching behavior of the transistor. Amplifier performances are also sensitive to the input driving waveform. That is why a class F driver is commonly used before it, in order to square the driving voltage.

The class E simulated here with a MWT770 Mesfet reaches 69.1% of efficiency when driven by a square signal. When the input signal is sinusoidal an efficiency of 59.3% is possible, at a drain supply of 2.5 V and an input power of 1 dBm, after an additional optimization.

Fig. 3 presents the alternation of current and voltage of the class E behavior. In comparison with ideal waveforms the lower efficiency is due to periods where current and voltage are both

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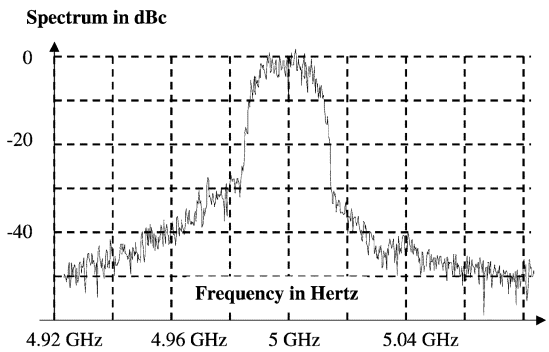

Fig. 2. 64-QAM Spectrum for $N = 32$ subcarriers considering cumulated imperfections.

TABLE I
EVM RESULTS FROM PREVIOUS STUDY

	N=32		N=128	
Imperfections/modulations	*16QAM*	*64QAM*	*16QAM*	*64QAM*
Phase noise (-95dBc)	4,43	4,46	4,5	4,54
Phase noise + IRR (-40dBc) + OLR (-36dBc)	4,64	4,69	4,76	4,81
VDD/PM	6,1	6,3	6,8	6,92
Phase noise + IRR + OLR + VDD/AM + VDD/PM + Time mismatch	**9,27**	**9,5**	**9,63**	**9,8**

TABLE II
EVM (% rms) RESULTS WHEN CLIPPING THE SIGNAL (IN dB RELATIVE TO AVERAGE ENVELOPE VALUE)

clipping in dB	16-QAM	64-QAM
-6	3,75	3,77
-9	1,64	1,65
-13	0,52	0,54
-14	0,4	0,4
-15	0,3	0,3
6	2,8	2,89
10	1,08	1,12

nonzero. By this way dc power consumption is created. This is due to the transistor nonideality.

Once the amplifier is designed, we have studied its compression and conversion effects introduced by this PA on the output signal (Fig. 4). The $\mathrm{V_{dd}/AM}$ response is consistent with the behavioral simulation previously made [4]. This default is small enough to be left un-corrected here. On the other hand, the phase shifting can be up to 80° for 3-V $\mathrm{V_{dd}}$ variation. This effect is due to the variation of drain to source capacitance and drain to source conductance in function of the drain voltage that shift the phase of the output signal. This strong nonlinearity is too much damageable on the signal transmission. This has to be corrected by a linearization techniques.

The $\mathrm{V_{dd}/PM}$ correction can be implemented either with digital or analog solution (thanks to voltage controlled phase shifter). The use of either one or the other solution depends on the signal frequency and realization technology. Designer choice will impact the final complexity and cost. In our simulation we interpolate the PA conversion response with a fourth-order polynomial equation as represented in Fig. 5. The opposite phase correction was then applied on the phase signal.

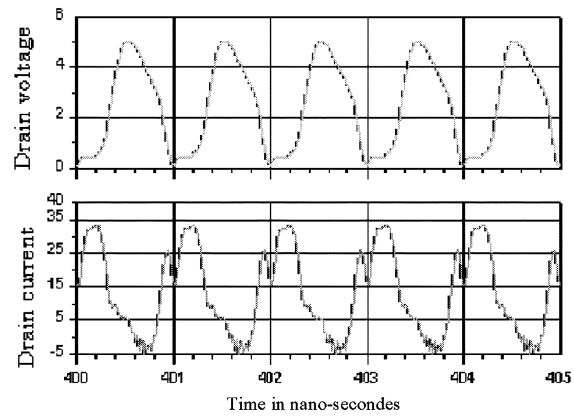

Fig. 3. Class E amplifier drain voltage and current variations at $\mathrm{VDS} = 2.5$ V for 1-dBm sinus input power.

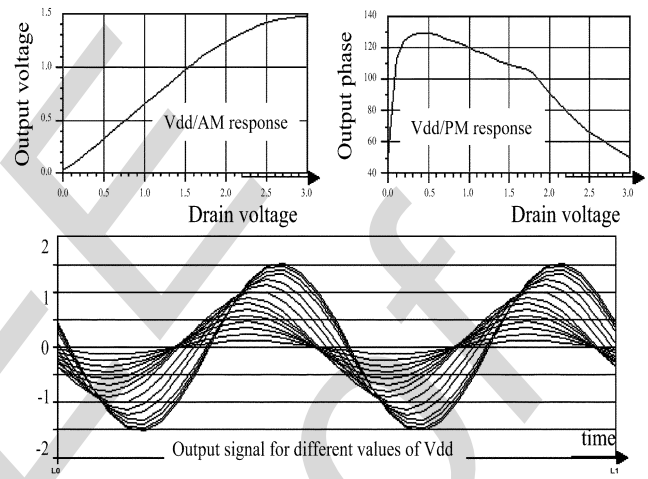

Fig. 4. $\mathrm{V_{dd}/AM}$ and $\mathrm{V_{dd}/PM}$ response, and time influence on output signal when driving with a sinusoidal input signal (1 dBm).

The maximum phase variation obtained with this correction is now reduced to 10° in the range 0.2 to 3.2 V (see Fig. 6).

IV. SIMULATION RESULTS

In order to reduce the dynamic of the envelope signal we choose to clip it. The clipping for low signal values is done in order to prevent a nearly-zero voltage supply of the PA. The clipping of high signal values is realized in order to limit the maximum voltage on the drain. We express clipping levels in dB relative to the average power of the envelope signal. In order to avoid a zero voltage or a too high value on the alimentation of the PA, we choose a clipping of -14 dB (0.2 V) and $+10$ dB (3.16) which causes respectively 0.4% and 1% EVM.

The output constellation after recombination is presented on Fig. 7. Results of simulation show a high EVM even with the phase correction (see Fig. 8).

We can clearly see that the conversion due to variation of the supply voltage is a major problem. Conversion effect impacts strongly the EVM with a noisy constellation. Results of EVM are reported in Table III. EVM results are too high to fulfil requirements such as Hiperlan2 with other imperfections added. This makes mandatory the compensation of conversion effects.

Spectrum regrowth is in the range of -30 dBc near the main channel. this is too high for OFDM standards such as IEEE 802.11a. The asymmetry of the spectrum observed is

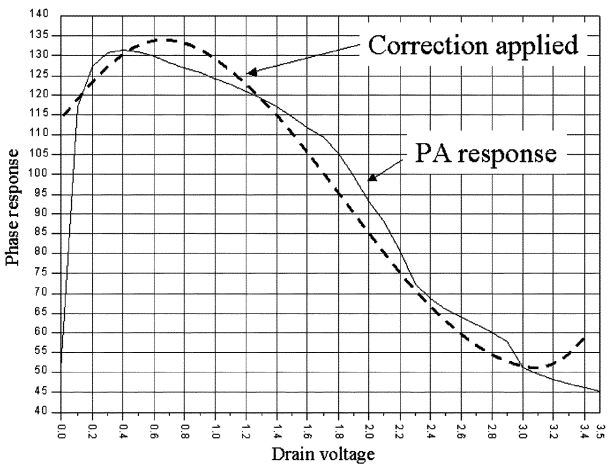

Fig. 5. Polynomial approximation of $\mathrm{V_{dd}/PM}$ conversion effect.

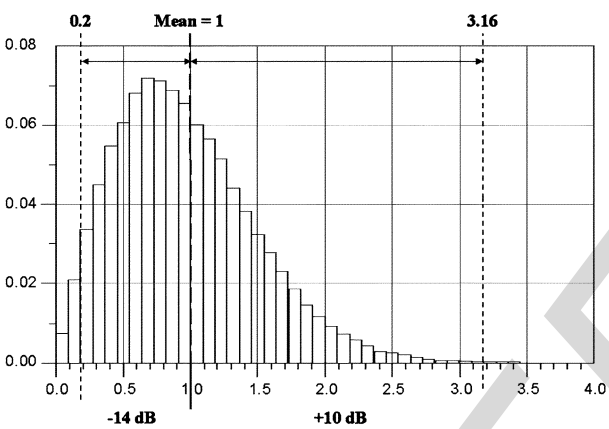

Fig. 6. Histogram of the envelope voltage, limits for the clipping.

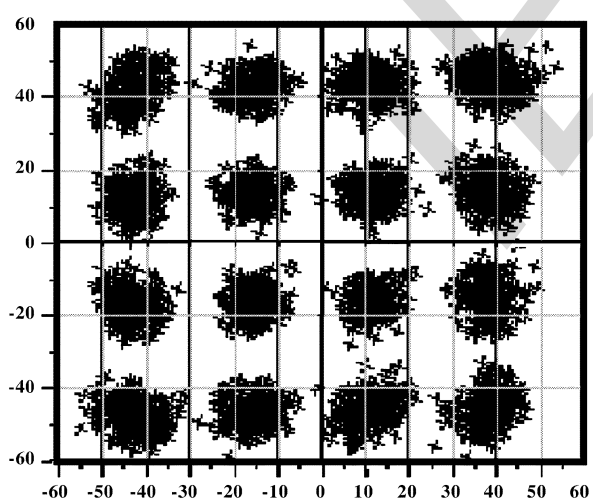

Fig. 7. Constellation received for $\mathrm{N} = 128$ sub-carriers.

due to conversion effect (frequency modulation implies Bessel distribution) evocated in [4]. Variation of the amplifier supply voltage creates an important conversion effect. The study of a phase correction (loop or predistortion) is necessary for the envelope restoration. Low phase conversion with supply variation is a design criterion for a class E amplifier. This concerns

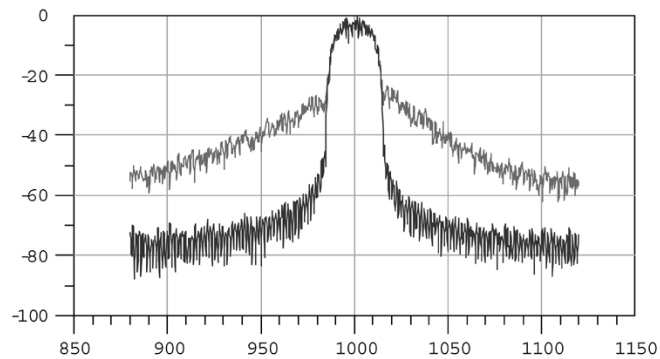

Fig. 8. Emitted spectrum of 64-QAM OFDM signal with $\mathrm{N} = 128$ subcarriers.

TABLE III
EVM RESULTS (MEAN/MAX IN % rms)

EVM mean and max in %rms	N=32	N=128
16-QAM	9,17 / 12,6	9,5 / 14
64-QAM	9,3 / 13	9,6 / 14

the switching behavior capability of the transistor (low output capacitance and conductance variation).

V. CONCLUSION

Using an EER architecture in order to design a linear OFDM emitter is subject to several imperfections. The most important are time mismatch, phase noise and conversion effect due to supply modulation of the PA. A synchronization loop is needed to achieve a mismatch lower than 5% of symbol duration. PLL synthesizer can attain low phase noise profile such as -95 dBc/Hz at 100 kHz.

In this paper the conversion effect is illustrated with a class E Mesfet amplifier. Results show the importance of correcting the $\mathrm{V_{dd}/PM}$ nonlinearity. This is possible in practice with a predistortion method but it increases the complexity of the transmitter. Designing a class E with low $\mathrm{V_{dd}/PM}$ (high FT and low output capacitance variation) and correction phase conversion are necessary in an EER OFDM transmitter.

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