

RESEARCH ARTICLE

Design of integrated all-pass filters with linear group delay for analog signal processing applications

João Alberto de França Ferreira¹ | Emilie Avignon-Meseldzija*¹ | Pietro Maris Ferreira¹ | Julien Sarrazin² | Philippe Bénabès¹

¹GeePs | Group of electrical engineering - Paris, CNRS, CentraleSupélec, Univ. Paris-Sud, Université Paris-Saclay, Sorbonne Université, Gif-sur-Yvette, France

²L2E | Laboratoire d'Électronique et Électromagnétisme, Sorbonne Université, Paris, France

Correspondence

* Emilie Avignon-Meseldzija
3 & 11 rue Joliot-Curie, Plateau de Moulon
91192 Gif-sur-Yvette CEDEX.
Email: emilie.avignon@centralesupelec.fr

Abstract

This article describes in detail the design of integrated linear group delay filters for analog signal processing (ASP) applications and their realization through constant-resistance lattice and bridged-T networks. Unlike previously published works, our design method uses a recursive procedure as the basis for the synthesis of a suitable transfer function. Thanks to this method, filters with a more linear group delay characteristic and flat magnitude response can be obtained. Two filters are designed in a 0.13 μm BiCMOS technology to demonstrate the method: a balanced lattice with a negative slope, and an unbalanced bridged-T of positive slope.

KEYWORDS:

all-pass filter, linear group delay, lattice, bridged-T, time-bandwidth product

1 | INTRODUCTION

The integration of an increasing number of functionalities has made portable electronic devices (PEDs) a necessity in modern life. The relevance of such devices is so significant that the global market for them is estimated at approximately 780 billion dollars by 2023¹. For PEDs, reliability, portability, and responsiveness are crucial requirements. These requirements generally translate into the need for low power integrated circuits (ICs) with low latency and high processing power. PEDs commonly employ digital signal processing (DSP) ICs due to their flexibility and reliability. However, DSP circuits face unprecedented challenges to comply with the requirements of real-time operation, higher operation frequencies, and low power consumption imposed by emerging applications. When operating at high-frequency ranges, like the decimeter, centimeter, and millimeter-wave bands, DSP circuits face significant difficulties, such as high power consumption, decreasing signal levels, and limited performances of interfacing data converters.

Analog signal processing (ASP) is an alternative or complementary approach to DSP. It enables circuits to perform real-time signal processing at higher operating frequencies and with lower power consumption. ASP requires filter devices with linear group delay to perform its fundamental operations: time stretching, time compression, and time reversal of signals². In the past, these filters were generally implemented through surface acoustic wave (SAW) devices^{3,4,5}. These devices have been used since the 1970s in areas such as communication systems, radars, and space exploration. However, their bandwidth and operating range, in the order of hundreds of MHz and a few GHz, respectively, do not conform anymore to the needs of newer applications. Besides, these devices present high insertion loss and require piezoelectric substrates. This late characteristic complicates their integration with modern semiconductor technologies, limiting their integration to system-in-package applications.

Recently, some attempts have been made to implement filters with linear group delay in modern semiconductor technologies. So far, the design methods have been based mainly on exploring the subbands of the filter where the group delay is approximately

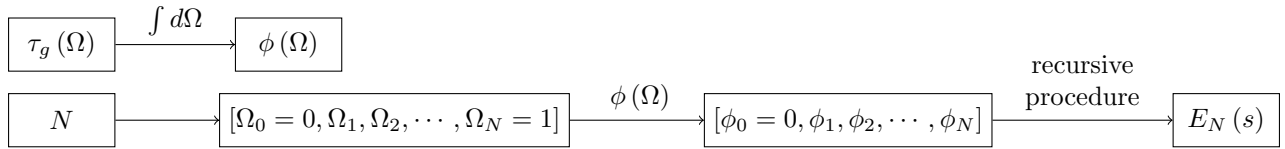


FIGURE 1 Flowgraph of the procedure to generate the all-pass prototype filter polynomial $E(s)$, starting from a specified group delay function $\tau_g(\Omega)$, where Ω is a normalized frequency, and filter order N .

linear⁶. Another method involves solving wave equations and computing the inverse Fourier transform⁷. In the present work, we introduce a new design approach, based on a recursive procedure originally reported by Henk⁸. To the author's knowledge, it is the first time that this method is applied in the design of integrated all-pass filters.

The design method is applied in the design of two all-pass filters in a 0.13 μm BiCMOS technology: one realized through a lattice network, and the other through a bridged-T network. The lattice filter has a negative slope linear group delay, while the bridged-T also has a linear group delay, but of positive slope. When compared to state of the art, both filters present an improved group delay linearity and flatter magnitude response. The explanation for the increased performance lies in the fact that specification is imposed since the earliest stage of the project, through the mathematical synthesis of the transfer function, in contrast to the approaches cited previously, where performance is the result of trade-off and optimization.

2 | TRANSFER FUNCTION GENERATION

The objective when designing an all-pass filter is to obtain the denominator and numerator polynomials of the filter transfer function, $E(s)$ and $P(s)$, respectively. The method explained in this article consists of generating the mentioned polynomials for an all-pass prototype filter and then frequency scaling the prototype filter transfer function. The procedure for generating the denominator polynomial was first proposed by Henk⁸ and is illustrated in Figure 1.

The designer starts by specifying the desired group delay function $\tau_g(\Omega)$ in the range $\Omega = 0$ to $\Omega = 1$, where Ω is a normalized frequency. The values 0 and 1 correspond to the limits of the operating band of the filter. The related phase function $\phi(\Omega)$ is obtained by integrating $\tau_g(\Omega)$ with respect to the normalized frequency. Then, a desired initial order N is specified for the filter. The prescribed filter order may be insufficient to generate the desired group delay characteristic. In this case, the designer can increase the prescribed order or modify the group delay specification.

The next step consists in creating a set of $N + 1$ normalized frequency values, where the lowest frequency value should be 0 and the highest 1. From this set of normalized frequency values, another set is created by evaluating $\phi(\Omega)$ for all the normalized frequency values of the previous set.

The transfer function denominator polynomial, $E(s)$, is generated by a recursive procedure given by^{8,9,10}

$$E_n(s) = \begin{cases} 1, & n = 0 \\ s + \alpha_0, & n = 1, \\ \alpha_{n-1} E_{n-1}(s) + (s^2 + \Omega_{n-1}^2) E_{n-2}(s), & n \geq 2 \end{cases} \quad (1)$$

where $0 \leq n \leq N$, and

$$\alpha_i = \begin{cases} \frac{\Omega_1}{\tan \phi_1}, & i = 0 \\ \alpha_{i-1} - \frac{\frac{\Omega_{i+1}^2 - \Omega_i^2}{\Omega_{i+1}^2 - \Omega_{i-1}^2}}{\alpha_{i-2} - \frac{\frac{\Omega_{i+1}^2 - \Omega_{i-2}^2}{\vdots}}{\alpha_0 - \frac{\Omega_{i+1}}{\tan \phi_{i+1}}}}, & i \geq 1 \end{cases} \quad (2)$$

The numerator polynomial, $P(s)$, is given by

$$P(s) = E(-s). \quad (3)$$

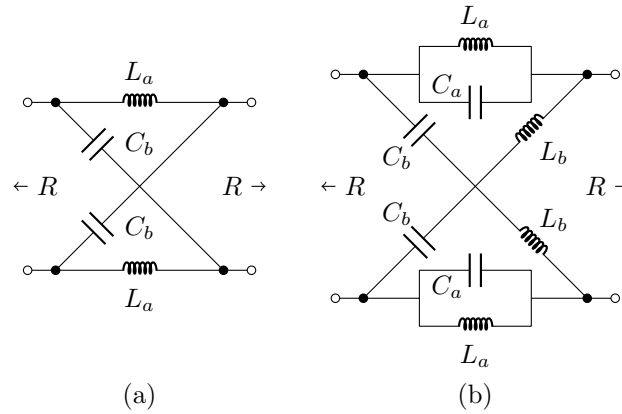


FIGURE 2 Lattice networks: (a) first-order section, (b) second-order section.

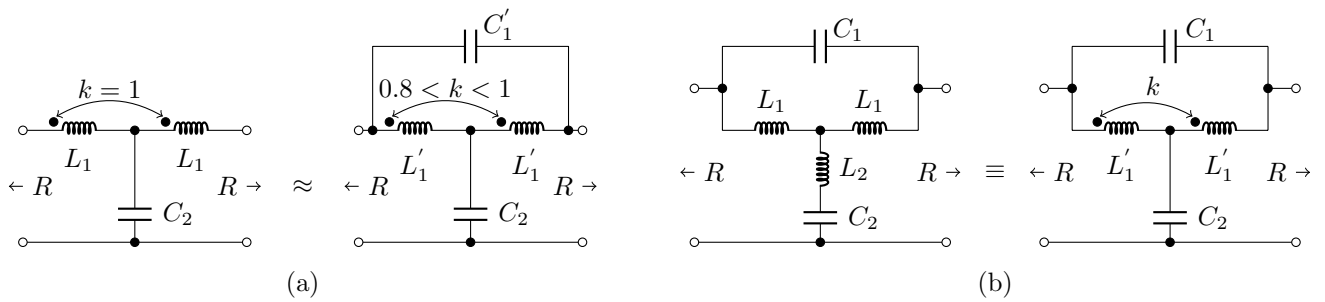


FIGURE 3 Bridged-T networks: (a) first-order section and approximate network to circumvent the need for ideal coupling, (b) second-order section.

The transfer function of the all-pass prototype filter is then given by

$$H(s) = \frac{P(s)}{E(s)} = \frac{E(-s)}{E(s)}. \quad (4)$$

3 | NETWORK SYNTHESIS PROCEDURE

Electronic filters are generally built by combining simple network sections. Two types of networks are usually used to realize passive all-pass filters, the lattice, and the bridged-T networks. The lattice network, illustrated in Figure 2, is a balanced network, while the bridged-T, shown in Figure 3, is its unbalanced equivalent. Both networks are examples of constant-resistance networks. They are highly versatile since their characteristic impedance is independent of their transmission properties¹¹.

The values of the components of a first- or second-order lattice section can be found from the coefficients of its transfer function. Alternatively, it can also be found through the real and imaginary parts of the roots of its transfer function—here noted as, respectively, σ_i and ω_i ¹².

- First-order section (A-section): $H(s) = \frac{c-s}{c+s}$

$$L_a = \frac{R}{c} = \frac{R}{\sigma_i}, \quad C_b = \frac{1}{Rc} = \frac{1}{R\sigma_i} \quad (5)$$

- Second-order section (B-section): $H(s) = \frac{s^2 - as + b}{s^2 + as + b}$

$$\begin{aligned} L_a &= \frac{Ra}{b} = \frac{2R\sigma_i}{\sigma_i^2 + \omega_i^2}, & C_a &= \frac{1}{Ra} = \frac{1}{2R\sigma_i} \\ C_b &= \frac{a}{Rb} = \frac{2\sigma_i}{R(\sigma_i^2 + \omega_i^2)}, & L_b &= \frac{R}{a} = \frac{R}{2\sigma_i} \end{aligned} \quad (6)$$

The lattice network can be converted into a bridged-T network through the use of the following relations:

- First-order section:

$$L_1 = \frac{L_a}{2}, \quad C_2 = 2C_b \quad (7)$$

- Second-order section:

$$C_1 = \frac{C_a}{2}, \quad C_2 = 2C_b \quad (8)$$

- Without coupling between coils ($k = 0$):

$$L_1 = L_a, \quad L_2 = \frac{L_b - L_a}{2} \quad (9)$$

- With magnetic coupling between coils:

$$L'_1 = \frac{L_a + L_b}{2}, \quad k = -\frac{L_b - L_a}{L_b + L_a} \quad (10)$$

In (9), a negative value for L_2 can arise if $L_b < L_a$. In this case, a magnetic coupling between the coils can be used to realize the section. In (10), a positive value for the coupling coefficient k means that the magnetic flows of both inductors combine. Otherwise, their magnetic flows are opposite.

In Figure 3, the position of the dots beside the inductors represents a positive value coupling coefficient, where the windings that form the inductors are wound in the same sense (clockwise-clockwise or counterclockwise-counterclockwise). By mirroring one of the inductors so that the dot appears on the other side, implies a change in the coupling coefficient signal, indicating that the inductors are now wound clockwise-counterclockwise to each other.

The first-order bridged-T section requires ideal coupling ($k = 1$), as shown in the left part of Figure 3a. In a practical implementation, the second-order bridged-T section at the right part of Figure 3a, with a coupling coefficient between 0.8 and 1, can be used to approximate a first-order section. The components values are given by¹³

$$C'_1 = \frac{C_a}{2} \frac{1-k}{1+k}, \quad L'_1 = \frac{L_a}{1+k}. \quad (11)$$

4 | DESIGN AND SYNTHESIS EXAMPLES

Different analog signal processing applications require filters with distinct group delay responses. For instance, a real-time Fourier transformer requires a linear response, while a spectrum sniffer requires a stepped response¹⁴. Aiming the realization of a real-time Fourier transform system, we present in this section two design examples: the first one of a lattice filter with a linear group delay of negative slope, and the second one of a bridge-T filter, also with a linear group delay, but of positive slope. In both examples, the specifications established for the prototype filters have the goal of maximizing the group delay swing and of approaching a perfect linear characteristic.

4.1 | Lattice Network with Linear Group Delay of Negative Slope

We should start the design of the filter by prescribing a desired group delay characteristic. The general expression for the linear group delay of a prototype filter is given by

$$\tau_g(\Omega) = A\Omega + \tau_0, \quad (12)$$

where Ω is the normalized frequency, A is the angular coefficient (which reflects the magnitude of the slope and its orientation, positive or negative), and τ_0 is a constant term that should be suitably chosen so as to assure the realizability of the filter.

Since we were interested in a filter with a high magnitude negative slope group delay, we started by defining an order four for the filter and setting a value of -1 for the angular coefficient. Then, based on the procedures explained in Section 2, we experimented with several values for the constant term until we found a value that generated a stable (realizable) transfer function with a linear group delay characteristic. Accomplished this, we increased the magnitude of the angular coefficient and again searched for a value for the constant term that would allow us to generate a stable transfer function with a group delay characteristic as linear as possible. This iterative process was carried out until it was no longer possible to obtain a stable transfer function with a sufficiently linear group delay characteristic without having to increase the filter order. Finally, the expression obtained for the group delay of the prototype filter and that was used in the filter design was

$$\tau_g(\Omega) = -4\Omega + 6.09. \quad (13)$$

The transfer function of the all-pass prototype filter obtained through the above procedure is given by (14), and it can be factored into first- and second-order terms (the transfer function of each section of the filter).

$$\begin{aligned} S_{21}(s) = \frac{P(s)}{E(s)} &= \frac{s^4 - 2.1168s^3 + 2.0175s^2 - 0.91681s + 0.15652}{s^4 + 2.1168s^3 + 2.0175s^2 + 0.91681s + 0.15652} \\ &= \frac{s^2 - 0.96164s + 0.23199}{s^2 + 0.96164s + 0.23199} \cdot \frac{s^2 - 1.1552s + 0.67471}{s^2 + 1.1552s + 0.67471} \end{aligned} \quad (14)$$

The poles and zeros of the transfer function are given in Table 1 and are used to verify if the filter is stable (all poles must lie on the left half of the complex plane) and to determine the component values of the lattice network. Accordingly, Table 2 presents the values of the components of the prototype lattice filter obtained through (6), as well as the values for the components when this prototype network is scaled to a frequency of 3.5 GHz and an impedance of 50 ohms. Figure 4a presents the filter schematic.

The group delay of each section composing the lattice prototype filter is shown in Figure 5, as well as the resultant group delay of the prototype filter. The pertinent frequency band is highlighted.

The scaled filter is implemented in STMicroelectronics BiCMOS9MW technology. The *cmim3p* metal-insulator-metal capacitor and the *indsym_lamw* planar inductor components of the technology were employed in the filter realization. The parameters values for the parameterized cells (PCells) are given in Table 3.

The forward transmission coefficient (S_{21}), the input reflection coefficient (S_{11}), and the group delay of the scaled filter are shown in Figure 6. In the figure, the dotted line represents a SPICE simulation considering the components with modeled intrinsic parasitics, but not considering interconnect parasitics. The continuous lines are the result of quasi-static electromagnetic

TABLE 1 Poles and zeros of (14).

Section	Poles	Zeros
1	$-0.4808202 - j0.0282478$	$0.4808202 - j0.0282478$
	$-0.4808202 + j0.0282478$	$0.4808202 + j0.0282478$
2	$-0.5775816 - j0.5840440$	$0.5775816 - j0.5840440$
	$-0.5775816 + j0.5840440$	$0.5775816 + j0.5840440$

TABLE 2 Values of components for the prototype lattice filter and its respective scaled network to a frequency of 3.5 GHz and an impedance of 50 ohms.

	Prototype		Scaled network	
	Section 1	Section 2	Section1	Section 2
L_a	4.145 H	1.712 H	9.425 nH	3.893 nH
C_a	1.040 F	0.866 F	945.7 fF	787.3 fF
C_b	4.145 F	1.712 F	3.770 pF	1.557 pF
L_b	1.040 H	0.866 H	2.364 nH	1.968 nH

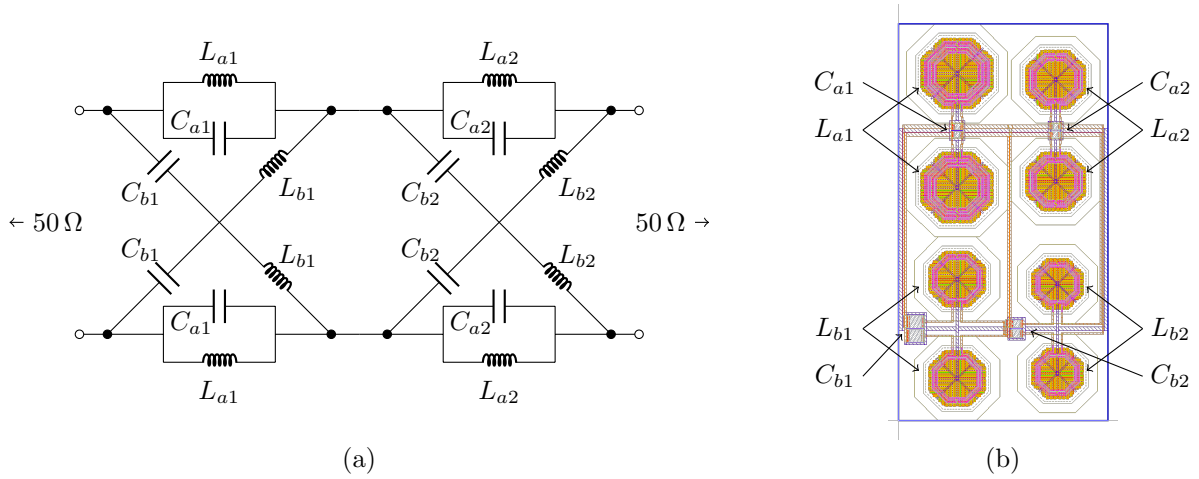


FIGURE 4 Lattice filter: (a) schematic (the values of components and PCell parameters are given in Tables 2 and 3, respectively), and (b) layout.

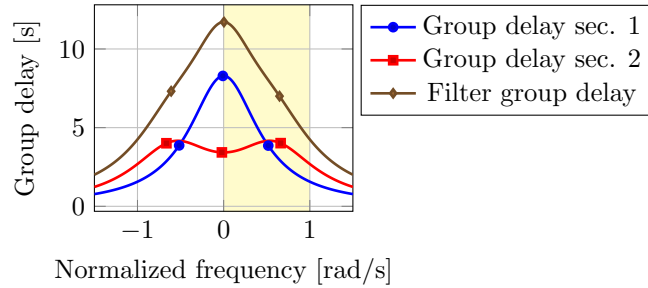


FIGURE 5 Group delay of each all-pass section and the resultant group delay characteristic of the prototype lattice filter, with the pertinent frequency band highlighted.

(EM) simulations of the complete filter layout (post-layout), where the blue line (RCTYP) represents nominal conditions, and the red (RCMIN) and green (RCMAX) lines represent the best- and worst-case corners, respectively. The EM simulations were performed using the *Momentum* simulator of the *Keysight ADS 2019* EDA tool¹⁵.

The filter presents a fairly linear group delay with a flat magnitude response. The maximum insertion loss is observed in the RCMAX corner and has a value of -4.38 dB at 2.9 GHz. The group delay swing ($\Delta\tau = \tau_{max} - \tau_{min}$) is greater than 300 ps for all corners, with the RCMIN corner presenting the smaller group delay slope, and the RCMAX presenting the biggest one. Since the

TABLE 3 Parameters values for the parameterized cells (PCells) used to realize the lattice filter.

	Internal diameter	No. of turns	Metal width	Capacitance	Width
Section 1					
L_a	134.465 μm	6	5 μm	C_a 945.7 fF	21.5 μm
L_b	127.045 μm	3	5 μm	C_b 3.770 pF	43.123 μm
Section 2					
L_a	123.57 μm	4	5 μm	C_a 787.3 fF	19.6 μm
L_b	108.935 μm	3	5 μm	C_b 1.557 pF	27.639 μm

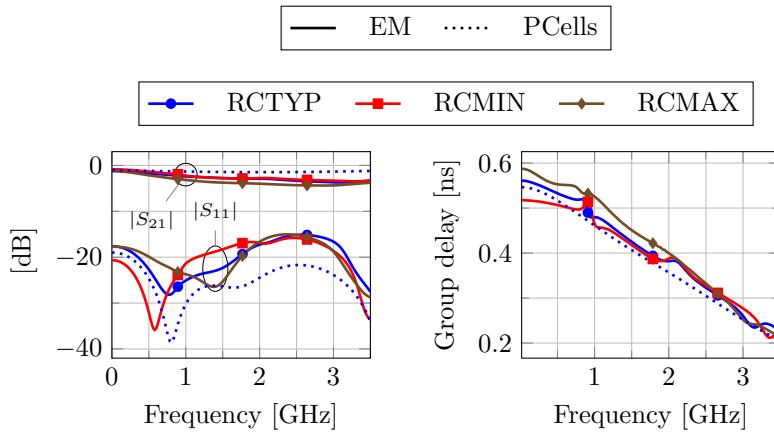


FIGURE 6 Frequency response and group delay of the scaled lattice filter.

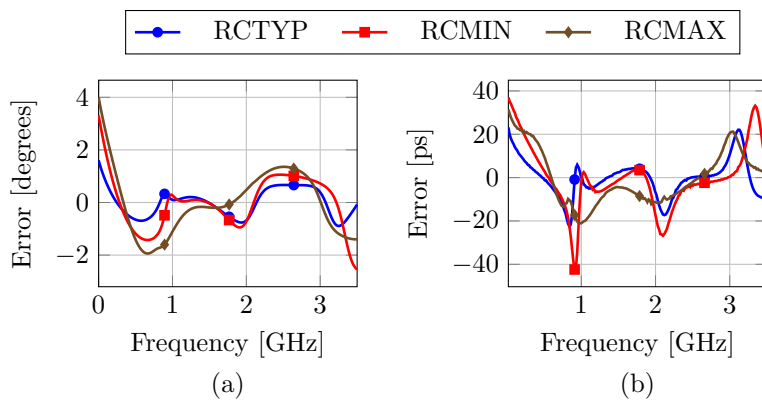


FIGURE 7 (a) Error in the lattice filter phase with respect to a second order polynomial regression curve calculated from its quasi-static EM simulation curve (200 points) and (b) Error in the lattice filter group delay with respect to a linear regression line calculated from its quasi-static EM simulation curve (200 points).

characteristics for the group delays given by the EM simulations of the complete layout diverges from the perfect characteristic obtained in the SPICE simulation, it can be inferred from Figure 6 that the imperfections in the linearity of the group delay are mainly due to interconnection parasitics.

To evaluate the deviation of the phase of the filter from its intended quadratic characteristic, we plot in Figure 7a the absolute error (in degrees) of the phase to a second-order polynomial regression curve calculated from the quasi-static EM simulation data (200 points). Similarly, to evaluate the linearity of the group delay, we plot in Figure 7b the absolute error (in picoseconds) of the group delay to a linear regression line calculated from the quasi-static EM simulation data (200 points). When working with linear phase filters, it is common to evaluate the flatness of the group delay through its relative error in percent. However, for a filter without a flat group delay, the relative error would be high in the band with a small delay, and small in the band with higher delay.

In Figure 7, the peaks in the plots coincide with the visible imperfections in the characteristics of the group delays presented in Figure 6. In the typical case (RCTYP), the phase error is smaller than one degree in practically the entire bandwidth, whereas for the group delay the error is smaller than twenty picoseconds, what represents around 6 % of the filter group delay swing.

Having the property of being a constant-resistance network, several filters can be cascaded without the need for matching networks. The insertion loss and group delay of the resultant cascade will be equal to the accumulation of the insertion losses and group delays of the different filters that constitute it. To ensure good power transfer and minimize signal reflection when cascading filters or connecting the filter to other circuits, it is important that the filter input and output impedances, respectively Z_{in} and Z_{out} , follow closely the reference impedance through all the passband, as the result presented in Figure 8, where the deviation of the input and output impedances relative to the 50 ohms reference impedance is maintained within a range of ± 10 ohms along the major part of the passband at all corners.

Figure 4 presents the lattice filter schematic and layout. The respective schematic components are indicated on the layout, and their values and PCell parameters are given in Tables 2 and 3, respectively. The layout dimensions are given in Table 8.

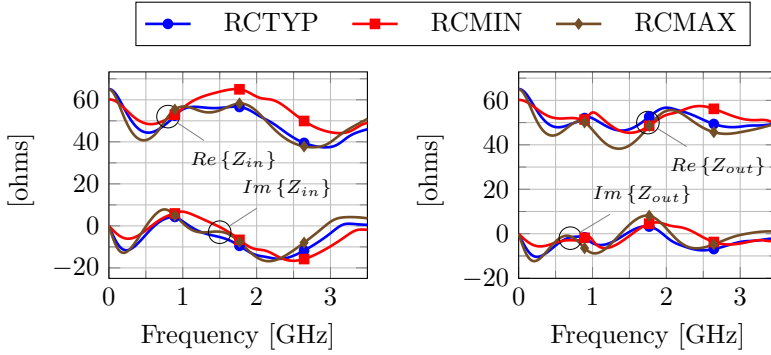


FIGURE 8 Real and imaginary parts of the input and output impedances of the lattice filter in nominal conditions (RCTYP), and for the RCMIN and RCMAX corners.

We summarize in Table 8 the major characteristics and performances in the state of the art of integrated filters with linear group delay. Except for the present work, all filters are composed of a cascade of distributed amplifiers (DAs) based transversal filters. The DAs are composed by two filters interconnected by active devices. These two filters form the gate and drain lines of the DAs. A typical performance used to evaluate filters presenting linear group delay is the time-bandwidth product (TBP or TBWP), consisting of the product of the filter group delay swing and bandwidth. As the filter group delay swing can be increased by increasing the filter order and/or by cascading filters, in an attempt to normalize and fairly compare the performance of the different filters, we divide its TBWP by the number of poles of the filter. From this, and thanks to the design method, it can be perceived that the designed lattice filter offers the higher TBWP per pole among all state of the art designs surveyed, while simultaneously presenting a flat magnitude response and fair group delay linearity.

4.2 | Bridged-T Network with Linear Group Delay of Positive Slope

A second fourth-order all-pass filter was designed, but this time with a group delay presenting a positive slope. The group delay specification is the same as in Ferreira et al.¹⁰ and is given by (15). Compared to (13), it is noticed that the present specification has a much smaller angular coefficient. This is because it is more difficult to obtain a perfectly linear characteristic for the group delay when it has a positive slope than when it has a negative slope. This fact had already been reported by Otto¹⁶.

$$\tau_g(\Omega) = \Omega + 2.5 \quad (15)$$

For this specification, the filter transfer function obtained by applying the procedures of Section 2 is given by

$$\begin{aligned} S_{21}(s) &= \frac{P(s)}{E(s)} = \frac{s^4 - 2.1408s^3 + 3.1524s^2 - 2.3190s + 0.90249}{s^4 + 2.1408s^3 + 3.1524s^2 + 2.3190s + 0.90249} \\ &= \frac{s^2 - 0.88794s + 1.3912}{s^2 + 0.88794s + 1.3912} \cdot \frac{s^2 - 1.2529s + 0.64873}{s^2 + 1.2529s + 0.64873} \end{aligned} \quad (16)$$

with its poles and zeros given in Table 4.

Table 5 presents, in its upper part, the values of the components for a bridged-T prototype filter with no coupling between coils calculated through (8) and (9) and the respective values of components for the scaled prototype to a frequency of 3.5 GHz (the $\Omega = 1$ normalized frequency is mapped to a frequency of 3.5 GHz) and an impedance of 50 ohms. The bottom part of Table 5 displays the values of the components for a bridged-T prototype filter presenting coupling between coils calculated with (8) and (10) and also the respective values of components for a bridged-T network scaled to the same frequency and impedance. For the

TABLE 4 Poles and zeros of (16).

Section	Poles	Zeros
1	$-0.4439706 - j1.0927244$	$0.4439706 - j1.0927244$
	$-0.4439706 + j1.0927244$	$0.4439706 + j1.0927244$
2	$-0.6264393 - j0.5062667$	$0.6264393 - j0.5062667$
	$-0.6264393 + j0.5062667$	$0.6264393 + j0.5062667$

TABLE 5 Values of components for: bridged-T prototype filters with and without coupling between coils; and their respective scaled networks (scaled to a frequency of 3.5 GHz and an impedance of 50 ohms).

	Bridged-T prototype		Scaled bridged-T network	
	Section 1	Section 2	Section 1	Section 2
Without coupling between coils ($k = 0$)				
C_1	0.563 F	0.399 F	512.1 fF	362.9 fF
L_1	0.638 H	1.931 H	1.451 nH	4.391 nH
L_2	0.244 H	-0.567 H	554.7 pH	-1.288 nH
C_2	1.277 F	3.863 F	1.161 pF	3.513 pF
With coupling between coils ($-1 \leq k \leq 1$ and $k \neq 0$)				
C_1	0.563 F	0.399 F	512.1 fF	362.9 fF
L'_1	0.882 H	1.365 H	2.006 nH	3.103 nH
k	-0.277	0.415	-0.277	0.415
C_2	1.277 F	3.863 F	1.161 pF	3.513 pF

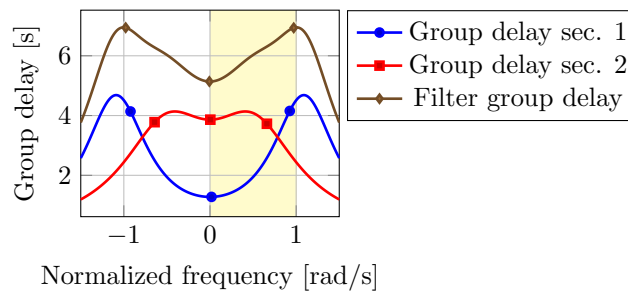


FIGURE 9 Group delay of each all-pass section and the resultant characteristics of the prototype bridged-T filter group delay, with the pertinent bandwidth highlighted.

filter that does not consider coupling between coils, the section 2 of the filter presents a negative value for the inductance of L_2 . That leads us to choose to implement this section through a network with a transformer (coupled inductors), which should exhibit a coupling factor of 0.415 between coils. Section 1 will be implemented through a network presenting no coupling between coils to avoid the burden of designing one more custom transformer. The filter was implemented using the same technology and PCells as the previous example, except for the custom transformer.

Figure 9 plots the group delay of each section that composes the bridged-T prototype filter and the filter resulting group delay, highlighting the relevant operating band.

The transformer necessary to realize the section 2 of the bridged-T filter was designed using the *Coilsys* utility¹⁷ of the *Keysight ADS 2019* EDA tool¹⁵. Its layout (c.f. Figure 11b) was then drawn in the *Cadence Virtuoso* platform¹⁸, where an electromagnetic simulation was performed to reveal the same characteristics obtained with the *ADS* tool. The inductance (L), series resistance (R_s) and quality factor (Q) of the primary and secondary inductors of the transformer, as well as the mutual inductance (M) and the coupling coefficient (k) between the inductors are shown in Figure 10, and were obtained through the relations (17) - (21)^{19,20,21,22}, based on the data of the EM simulation of the testbench of Figure 11a.

The self-resonant frequencies of the inductors are at about 7.9 GHz, too close to allow a constant inductance value, as can be verified in Figure 10a. At the upper limit of the frequency band, the deviation in the inductance value from its ideal value of 3.103 nH is almost 13%. The series resistance, presented in Figure 10b, is significant, what results in a small quality factor (c.f. Figure 10c), despite the use of a thick metal line (3 μm) in parallel with the top aluminum cap available in the technology.

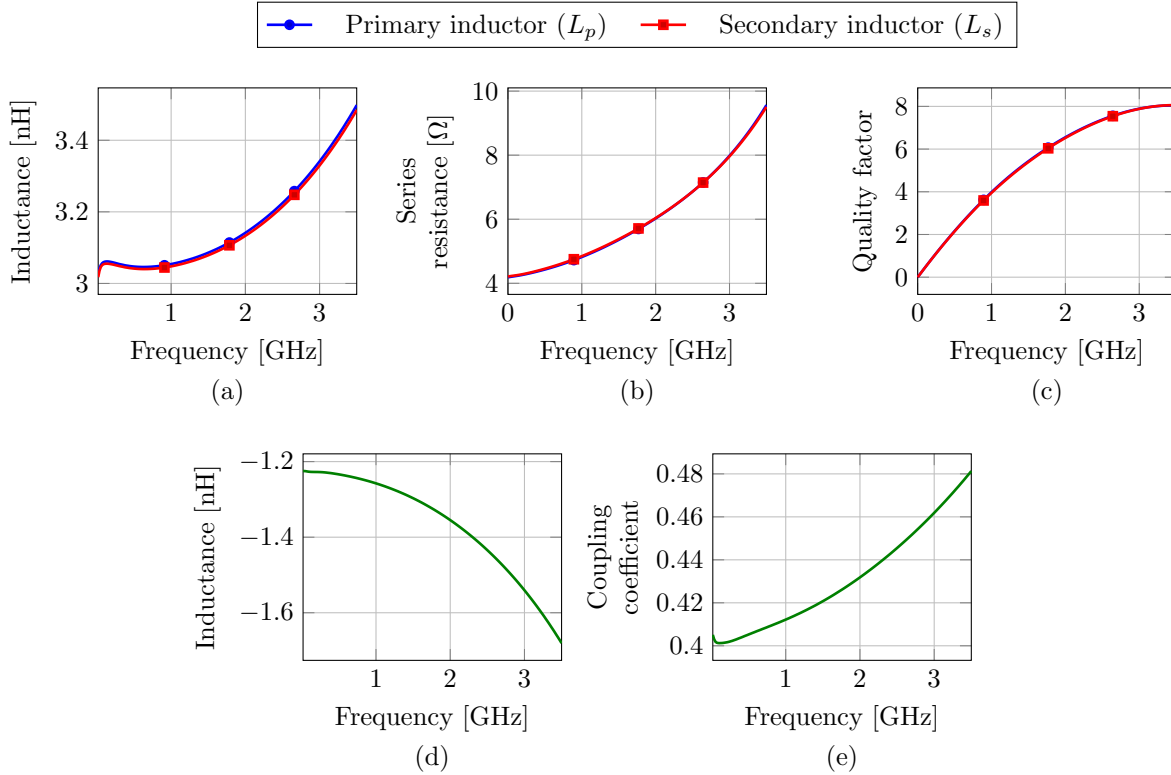


FIGURE 10 Coupled inductors characteristics: (a) inductances, (b) series resistances, (c) quality factors, (d) mutual inductance, and (e) coupling coefficient.

The coupling coefficient deviates from its intended value of 0.415 as the frequency increases, reaching a deviation of 15 % at the upper limit of the frequency band.

$$L_p = \frac{\text{Im}\{Z_{11}\}}{2\pi f}, \quad L_s = \frac{\text{Im}\{Z_{22}\}}{2\pi f} \quad (17)$$

$$R_{s_p} = \text{Re}\{Z_{11}\}, \quad R_{s_s} = \text{Re}\{Z_{22}\} \quad (18)$$

$$Q_p = \frac{\text{Im}\{Z_{11}\}}{\text{Re}\{Z_{11}\}}, \quad Q_s = \frac{\text{Im}\{Z_{22}\}}{\text{Re}\{Z_{22}\}} \quad (19)$$

$$M = \frac{\text{Im}\{Z_{21}\}}{2\pi f} \quad (20)$$

$$k = -\frac{M}{\sqrt{L_p L_s}} = -\frac{\text{Im}\{Z_{21}\}}{\sqrt{\text{Im}\{Z_{11}\} \text{Im}\{Z_{22}\}}} \quad (21)$$

A transformer with interleaved structure and rectangular shape was implemented to ease the layout task. The dimensions of the designed transformer are given in Table 6.

The scaled bridged-T filter was implemented in the same technology using the same PCells used in the lattice example. The PCells parameters values are given in Table 7.

Figure 12 presents the nominal quasi-static EM simulation as well as the RCMIN and RCMAX corners simulations for the forward transmission coefficient (S_{21}), the input reflection coefficient (S_{11}) and the group delay of the scaled bridged-T filter. As expected, the RCMIN corner presents the best frequency response and the most linear group delay as, in this case, the parasitics are minimized. The RCMAX corner displays the worst frequency response and group delay linearity, with the nominal RCTYP

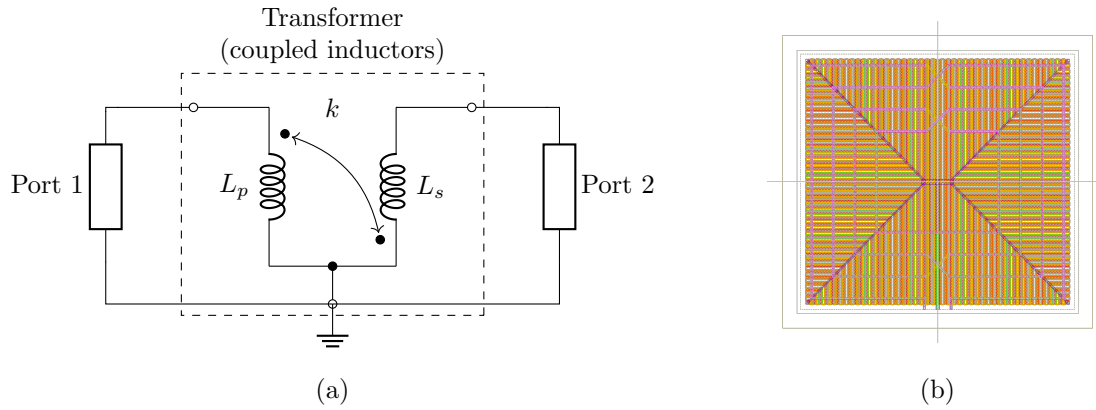


FIGURE 11 Transformer: (a) transformer schematic and respective testbench for extracting the parameters exhibited in Figure 10, (b) layout.

TABLE 6 Designed transformer dimensions.

Line width	Line space	Turns	Internal dimensions
5 μm	40 μm	4	200/250 μm

TABLE 7 Parameters values of the components of the technology (PCells) for the bridged-T filter.

	Internal diameter	No. of turns	Metal width	Capacitance	Width
Section 1					
L_1	84.145 μm	3	5 μm	C_1 512.1 fF	15.77 μm
L_2	69.945 μm	2	5 μm	C_2 1.161 pF	23.83 μm
Section 2					
L'_1	refer to Table 6			C_1 362.9 fF	13.01 μm
				C_2 3.513 pF	40.3 μm

case in between the RCMIN and RCMAX performances. The insertion loss is better than -4.14 dB, observed at 3.5 GHz for the RCMAX corner, while the group delay swing is about 60 ps.

Figure 13a plots, for the three corners (RCTYP, RCMIN, and RCMAX), the deviation (in degrees) of the phase of the filter from a second-order polynomial regression curve calculated from the quasi-static EM simulation data (200 points) representing the ideal quadratic phase characteristic. Figure 13b, on its turn, plots the deviation (in picoseconds) of the group delay of the filter from a linear regression line calculated from the quasi-static EM simulation data (200 points) representing the idealized linear group delay. The phase deviation is smaller than 1.35 degrees for the RCMAX corner, and 0.5 degrees for the RCMIN corner, whilst the group delay deviates a maximum of 11.83 ps for the RCMAX corner and 3.38 ps for the RCMIN corner.

The real and imaginary parts of the input and output impedances of the bridged-T filter are plotted in Figure 14. Similar to the lattice filter, the bridged-T filter input and output impedances are maintained within a range of about ± 10 ohms around the reference impedance of 50 ohms for the major part of the passband at all corners. When cascading N filters, the group delay swing will be multiplied by N . As a side effect, the small mismatches between the cells may introduce non-linearities in the group delay characteristic. This problem must then be addressed in the layout.

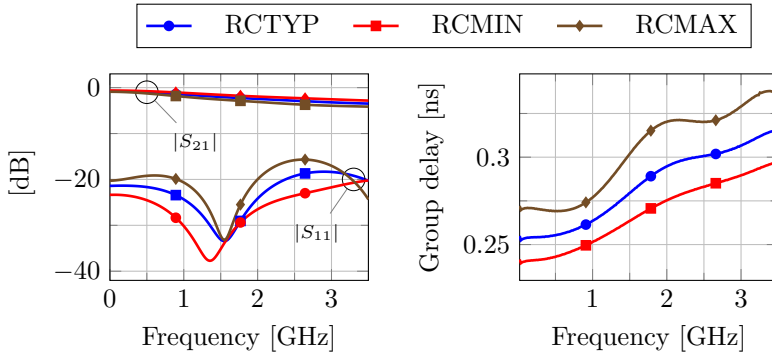


FIGURE 12 Frequency response and group delay of the scaled bridged-T filter.

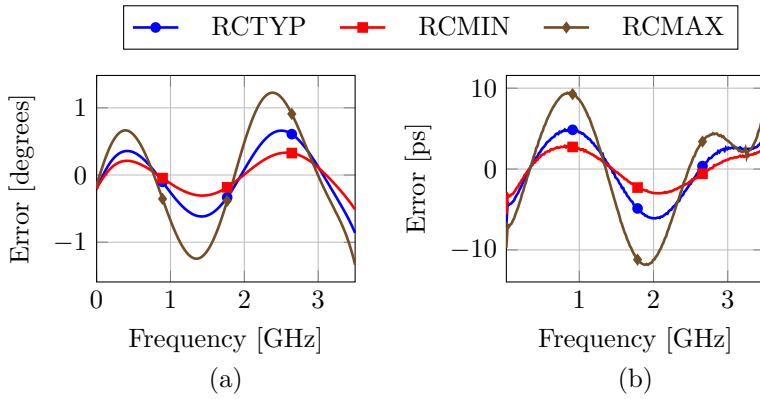


FIGURE 13 (a) Error on the phase of the bridged-T filter related to a second-order polynomial regression curve calculated from its quasi-static EM simulation curve (200 points) and (b) Error on the group delay of the bridged-T filter related to a linear regression line calculated from its quasi-static EM simulation curve (200 points).

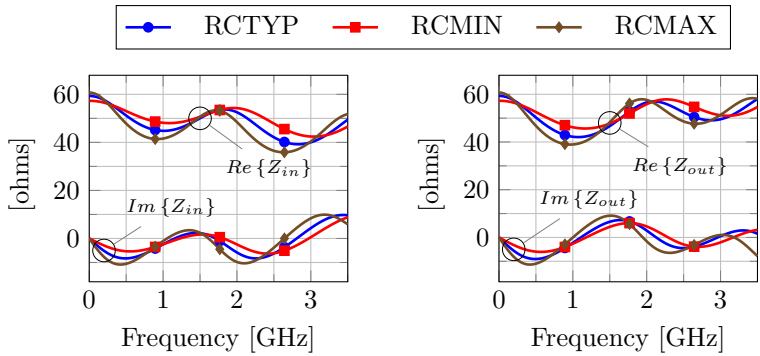


FIGURE 14 Real and imaginary parts of the input and output impedances for the scaled bridged-T filter.

Figure 15 presents the bridged-T filter schematic and layout. The corresponding schematic components are indicated on the layout, and their values are given in Table 5, while the respective PCell technology parameters are presented in Table 7. The layout dimensions are given in Table 8.

In Table 8, that summarizes the principal characteristics and performances in the state of the art of integrated filters with linear group delay, we highlight that the designed lattice and bridged-T filters present, simultaneously, a fair group delay linearity with a flat magnitude response, besides being the first passive filters being reported.

5 | CONCLUSION

This article presented the detailed design of two integrated all-pass filters with linear group delays for analog signal processing applications. Unlike previously published works, the designed filters were obtained through the mathematical synthesis of a suitable transfer function. The benefit of this design methodology is that the resulting integrated filters present better linearity

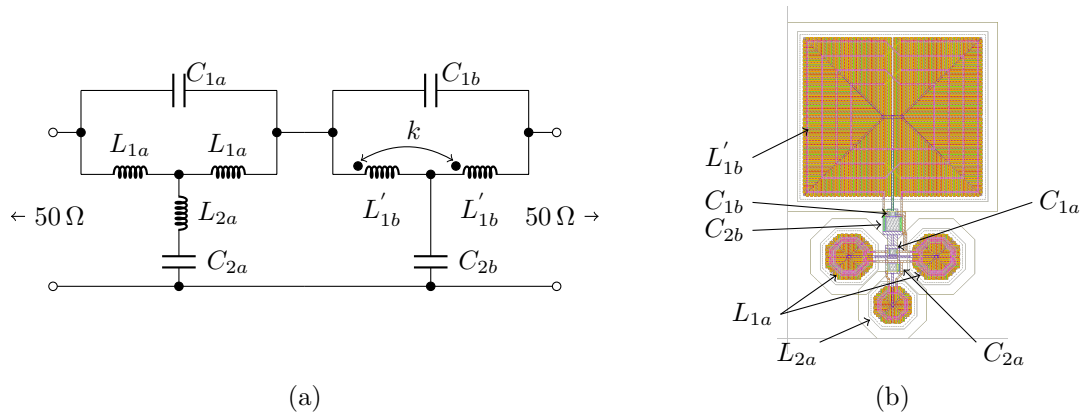


FIGURE 15 Bridged-T filter: (a) schematic (the values of components and PCell parameters are given in Tables 5 and 7, respectively), and (b) layout.

TABLE 8 Comparison of state of the art integrated linear group delay filters.

	Xiang et al. ²³	Xiang et al. ^{24,25}	Xiang et al. ⁷	Salvucci et al. ⁶	This work (lattice)	This work (bridged-T)
Technology	0.13 μm CMOS	0.13 μm CMOS	0.13 μm CMOS	0.25 μm GaN MMIC	0.13 μm BiCMOS	
Size	1.5 mm x 4.7 mm	1 mm x 4.5 mm	2 x 1.6 mm x 5 mm	3.7 mm x 4.2 mm	686 μm x 1330 μm (without pads)	646 μm x 998 μm (without pads)
Bandwidth	11 GHz to 15 GHz	12 GHz to 16 GHz	0.4 GHz to 4 GHz	8 GHz to 12 GHz	0 GHz to 3.5 GHz	
Fractional bandwidth	31 %	29 %	164 %	40 %	200 %	
Group delay slope	positive	positive	negative	positive	negative	positive
Group delay swing	0.8 ns	1.5 ns	1.2 ns	0.6 ns	0.33 ns	60.6 ps
TBWP	3.2	6	5	2.4	1.155	0.212
Number of poles	30	30	44	40	4	4
TBWP/pole	0.107	0.200	0.114	0.060	0.289	0.053
Power consumption	active	active	750 mW	2.47 W	passive	passive
Group delay linearity	poor	poor	fair	poor	fair	fair
Gain flatness	poor	poor	poor	good	good	good

and a flatter magnitude response when compared to state of the art. The integrated technology used for implementation was the BiCMOS9MW from STMicroelectronics. One filter has a negative group delay slope and the other, a positive group delay slope.

References

1. Portable Electronics Market Research Report - Global Forecast 2023. <https://www.marketresearchfuture.com/reports/portable-electronics-market-4126>. Accessed on: June 12, 2019.
2. Caputi WJ. Stretch: A time-transformation technique. *IEEE Trans. Aerosp. Electron. Syst.* 1971; AES-7(2): 269–278. doi: 10.1109/TAES.1971.310366
3. Morgan DP, Ash EA. Acoustic-surface-wave dispersive delay line. *Proc. Inst. Electr. Eng.* 1969; 116(7): 1125–1134. doi: 10.1049/piee.1969.0212
4. Gerard HM, Smith WR, Jones WR, Harrington JB. The design and applications of highly dispersive acoustic surface-wave filters. *IEEE Trans. Microw. Theory Techn.* 1973; 21(4): 176–186. doi: 10.1109/TMTT.1973.1127968
5. Jack MA, Grant PM, Collins JH. The theory, design, and applications of surface acoustic wave Fourier-transform processors. *Proc. IEEE* 1980; 68(4): 450–468. doi: 10.1109/PROC.1980.11674

6. Salvucci A, Colangeli S, Palomba M, Polli G, Limiti E. An active dispersive delay line in GaN MMIC technology for X-band applications. In: *21st International Conference on Microwave, Radar and Wireless Communications*. IEEE; May 9-11, 2016; Krakow, Poland: 1–4
7. Xiang B, Wang X, Apsel AB. On-chip demonstration of real time spectrum analysis (RTSA) using integrated dispersive delay line (IDDL). In: *IEEE MTT-S International Microwave Symposium Digest*. IEEE; June 2-7, 2013; Seattle, WA, USA: 1–4
8. Henk T. The generation of arbitrary-phase polynomials by recurrence formulae. *Int. J. Circuit Theory Appl.* 1981; 9(4): 461–478. doi: 10.1002/cta.4490090407
9. Zhang Q, Sounas DL, Caloz C. Synthesis of cross-coupled reduced-order dispersive delay structures (DDSs) with arbitrary group delay and controlled magnitude. *IEEE Trans. Microw. Theory Techn.* 2013; 61(3): 1043–1052. doi: 10.1109/TMTT.2013.2241785
10. Ferreira JAF, Avignon-Meseldzija E, Ferreira PM, Bénabès P. Design and Synthesis of Arbitrary Group Delay Filters for Integrated Analog Signal Processing. In: *25th IEEE International Conference on Electronics, Circuits and Systems*. IEEE; December 9-12, 2018; Bordeaux, France: 613–616
11. Zverev AI. *Handbook of Filter Synthesis*. Baltimore, MD, USA: John Wiley & Sons . 1967.
12. Matthes H. Designing high-grade delay equalizers. *NTZ-CJ* 1965(4): 177–185.
13. Hajek K, Sedlacek Z, Sviezeny B. New circuits for realization of the 1st and 2nd order all-pass LC filters with a better technological feasibility. In: *Proceedings of the 2002 IEEE International Symposium on Circuits and Systems*. IEEE; May 26-29, 2002; Phoenix-Scottsdale, AZ, USA: III–523–III–526
14. Caloz C, Gupta S, Zhang Q, Nikfal B. Analog signal processing: A possible alternative or complement to dominantly digital radio schemes. *IEEE Microw. Mag.* 2013; 14(6): 87–103. doi: 10.1109/MMM.2013.2269862
15. Advanced Design System (ADS) | Keysight (formerly Agilent's Electronic Measurement). <https://www.keysight.com/en/pc-1297113/advanced-design-system-ads?cc=US&lc=eng>. Accessed on: May 14, 2019.
16. Otto OW. The chirp transform signal processor. In: *1976 Ultrasonics Symposium*. IEEE; September 29-October 1, 1976; Annapolis, MD, USA: 365–370
17. CoilSys Demo for ADS 2017 - YouTube. https://www.youtube.com/watch?v=nos_fjcic-Y. Accessed on: May 14, 2019.
18. Virtuoso Layout Suite. https://www.cadence.com/content/cadence-www/global/en_US/home/tools/custom-ic-analog-rf-design/layout-design/virtuoso-layout-suite.html. Accessed on: June 17, 2019.
19. Luong HC, Yin J. Transformer Design and Characterization in CMOS Process. In: *Transformer-Based Design Techniques for Oscillators and Frequency Dividers*. Cham: Springer International Publishing. 2016 (pp. 7–19)
20. Mohan SS. *The design modeling and optimization of on-chip inductor and transformer circuits*. Doctoral thesis. Stanford University, 1999.
21. Leite B. *Design and modeling of mm-wave integrated transformers in CMOS and BiCMOS technologies*. Doctoral thesis. Université Bordeaux 1, 2011.
22. Leite B, Kerherve E, Begueret JB, Belot D. Design and characterization of CMOS millimeter-wave transformers. In: *SBMO/IEEE MTT-S International Microwave and Optoelectronics Conference*. IEEE; November 3-6, 2009; Belém, Brazil: 402–406
23. Xiang B, Kopa A, Apsel AB. A novel on-chip active dispersive delay line (DDL) for analog signal processing. *IEEE Microw. Compon. Lett.* 2010; 20(10): 584–586. doi: 10.1109/LMWC.2010.2064761

24. Xiang B, Kopa A, Fu Z, Apsel AB. An integrated Ku-band nanosecond time-stretching system using improved dispersive delay line (DDL). In: *Paper Digest of the 2012 IEEE 12th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems*. IEEE; January 16-18, 2012; Santa Clara, CA, USA: 151–154
25. Xiang B, Kopa A, Fu Z, Apsel AB. Theoretical analysis and practical considerations for the integrated time-stretching system using dispersive delay line (DDL). *IEEE Trans. Microw. Theory Techn.* 2012; 60(11): 3449–3457. doi: 10.1109/TMTT.2012.2215623

How to cite this article: J. A. de F. Ferreira, E. Avignon-Meseldzija, P. M. Ferreira, and P. Bénabès (2019), Design of integrated all-pass filters with linear group delay for analog signal processing applications, *Int. J. Circ. Theor. Appl.*, 2019;00:1–16.