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A statistical analysis of the temperature coefficients of industrial silicon solar cells

Salvador Ponce-Alcántara[a*], James Patrick Connolly[a], Guillermo Sánchez[a], José Manuel Míguez[b], Volker Hoffmann[c], Ramón Ordás[b]

[a]*Valencia Nanophotonics Technology Center, Universitat Politècnica de València, 46022, Spain*
[b]*Silicio FerroSolar S.L., Polígono Industrial de Sabón,Arteixo, A Coruña, 15142, Spain*
[c]*V.Hoffmann Technology Consulting, Rethelstr. 8, 12435 Berlin, Germany*

Abstract

This paper presents an experimental study of the variation in the performance of silicon solar cells with temperature. The cells studied were fabricated from standard electronic grade and upgraded metallurgical grade silicon. Both monocrystalline and multicrystalline silicon wafers are included. The main object is to evaluate critical cell parameters for cell performance against temperature. The critical parameters selected are the wafer type, wafer resistivity, fabrication process routing, and solar cell electrical parameters. Their impact on cell performance is evaluated by systematic study expressed in terms of temperature coefficients. The resulting quantitative study finds different cell performance sensitivities to specific parameters: the crystal growth, the use of electronic grade or upgraded metallurgical grade silicon wafers, and the fabrication process employed. It is shown that the temperature coefficient of the short circuit current is an important factor in the tendency of the temperature coefficient of the maximum power. This phenomenon is responsible for the superior temperature coefficient observed in solar cells fabricated from upgraded metallurgical grade silicon wafers. Furthermore, the study quantitatively demonstrates the sensitivity of cell temperature coefficient to fabrication process. The optimum process for a superior temperature coefficient is identified, and also corresponds to an improved overall efficiency.

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Keywords: Solar cells; Temperature coefficient; UMG-silicon

* Corresponding author. Tel.: +34 96 387 7000; fax: +34 96 387 7827.
E-mail address: salponce@ntc.upv.es

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1. Introduction

The characterization of solar cells under standard test conditions is performed at 25ºC. However, operational temperatures may depart significantly from that value in photovoltaic (PV) installations. Operational conditions depend mainly on illumination level, outdoor temperature, wind speed, location of the PV module, and its capacity to dissipate the heat generated. It is therefore important to take in account the temperature coefficients (CT) of the solar cell in order to predict the real power that can be produced in an installation under operating conditions. For example, at a nominal operating temperature of T = 45ºC the temperature dependence of maximum power output (Pmpp) can be linearly parameterized in terms of its temperature coefficient (CT Pmpp) and the power output in standard test conditions as follows:

$$\mathrm{Pmpp\ (T)} = \mathrm{Pmpp}(25^{o}\mathrm{C}) \cdot (1 + \mathrm{CT\ Pmpp}(\mathrm{T} - 25^{o}\mathrm{C})) \quad (1)$$

This maximum output power of a standard silicon PV module increases by 0.66% if the CT Pmpp changes from -0.45%/ºC to -0.42%/ºC.

Despite the actual reduction in the silicon wafer price, it still represents around 35% of the total cost of a PV module [1]. Consequently, given current industrial fabrication processes, solar cells fabricated from upgraded metallurgical grade silicon (UMG-Si) substrates are becoming more common due to their comparable efficiencies with respect to the electronic grade silicon (EG-Si) solar cells together with their lower cost.

One interesting issue with the solar cells processed with the UMG-Si substrate is the behavior as a function of temperature. There are a number of publications presenting a study of the temperature coefficients of solar cells respect to the substrate type (UMG-Si versus EG-Si) [2] or its resistivity [3]. These publications find that the CT Pmpp of solar cells made from UMG-Si is lower than that of standard cells made from EG-Si, due notably to the strong improvement of the photocurrent with increasing temperature. Furthermore, the temperature coefficients are well anticorrelated to the solar cell resistivity.

The fabrication process has a notable influence on both the electrical parameters and the CT of the solar cells [4]. High efficiency fabrication processes produce solar cells with a high open circuit voltage (Voc) and power. In addition to this, an almost linear relationship has been demonstrated between the Voc and the CT Pmpp [5].

Following these considerations, the work presented in this paper analyses the temperature coefficients of solar cells processed in different fabrication lines with EG and UMG mono and multicrystalline silicon (mc-Si) wafers with different resistivities.

2. Temperature effects on the electrical parameters of silicon solar cells

As with any other electronic device, the temperature affects the performance of solar cells. An increase in temperature generally leads to a decrease in the power for a number of reasons which are going to be reviewed in the following sections. As a consequence of the temperature variation, the band gap energy changes according to the equation giving by Varshni [6]:

$$\mathrm{E_g(T)} = \mathrm{E_g(0)} - \frac{\alpha \mathrm{T}^2}{\mathrm{T} + \beta} \quad (2)$$

where Eg (T) is the band gap of the semiconductor at a temperature T, Eg (0) is its value at 0 K, and α and β are constants which depend on the semiconductor material.

According to the equation (2), the band gap decreases if temperature increases. Because of this, the short circuit current of a solar cell generally increases with temperature due to the possibility of absorbing photons with lower energies to create e-h pairs [7]. On the other hand, there is a reduction in built-in junction potential and hence in Voc, and in efficiency, as the silicon band gap moves further away from the optimum of 1.35eV for a one sun AM1.5G spectrum.

The mobility of electrons depends on temperature as well, decreasing with temperature. When the temperature increases, atoms will vibrate more and hinder the electrons passing through the lattice. This is phonon or thermal

scattering, and is responsible of the limitation on the carrier mobility in EG cells [2] at temperatures at and above standard test conditions.

The mobility of electrons is also affected by the content of impurities, decreasing lightly with them.

$$\frac{1}{\mu(T)} = \frac{1}{\mu_{phonon}(T)} + \frac{1}{\mu_{impurity}(T)} \tag{3}$$

On the other hand, the large content of ionized impurities in the UMG-Si wafers compared to EG-Si wafers produces a weaker mobility reduction with increasing temperature [2,8]. Therefore, the temperature coefficient of the short circuit current density (CT Jsc) is higher in UMG-Si solar cells.

Another factor to take into account in the variation of the short circuit current density is the dependence of the Shockley Read Hall (SRH) recombination and lifetime with temperature. This type of recombination is dominant in industrial silicon wafers, and therefore, it has a significant influence on the effective lifetime.

Compensation in UMG-Si wafers is known to produce an increase in their effective lifetime [9], a parameter which is correlated with the Jsc. This increment on the lifetime is stronger with temperature, and has a larger influence on the Jsc than the weak reduction of mobilities.

The open circuit voltage can be expressed as:

$$Voc = \frac{kT}{q} \ln\left(\frac{Jsc}{Jo} + 1\right) \tag{4}$$

where kT/q is the thermal voltage and Jo the dark saturation current density. For high Voc, a low Jo is absolutely necessary.

The temperature dependence of Voc can be obtained from Eq. (4) as:

$$\frac{dVoc}{dT} = \frac{Voc}{T} + \frac{kT}{q}\left(\frac{1}{Jsc}\frac{dJsc}{dT} - \frac{1}{Jo}\frac{dJo}{dT}\right) \tag{5}$$

As a function of the band gap, the variation of the Voc with temperature can be expressed as [10]:

$$\frac{dVoc}{dT} \approx \frac{dE_g/q}{dT} + \frac{Voc - E_g/q}{T} \tag{6}$$

Examining the functional form of equations (5) and (6), it is deduced a trend which is that the reduction in Voc with temperature is lower in the case of higher Voc values. Besides, Voc decreases with temperature due to a reduction of the band gap, whereas the dark saturation current density increases with temperature due to the increment in the carrier concentration. Jo is highly sensitive to temperature changes. Because of that, higher Jo implies lower Voc and higher variations of the Voc with temperature.

The Fill Factor temperature coefficient (CT FF) can be defined as [11]:

$$\frac{1}{FF}\frac{dFF}{dT} = (1 - 1.02FF_o)\left(\frac{1}{Voc}\frac{dVoc}{dT} - \frac{1}{T}\right) - \frac{R_s}{\left(\frac{Voc}{Isc} - R_s\right)}\left(\frac{1}{R_s}\frac{dR_s}{dT}\right) \tag{7}$$

where FF_o is the idealized FF without series resistance and R_s is the cell series resistance. Therefore, higher variations of the CT Voc imply higher changes on the FF with temperature. Furthermore, silicon solar cells with lower FF due to higher Rs are expected to have a worse dependence of FF with temperature.

3. Experimental study

Mono and multicrystalline p-type silicon wafers from different suppliers have been processed in several industrial fabrication lines with a phosphorus emitter and an aluminum back surface field. The wafer sizes are 156 x 156 mm and a diameter of 200 mm for the monocrystalline Czochralski (Cz) samples, and 156 x 156 mm for the quasi-mono and multicrystalline silicon wafers. The resistivities range between 0.5 and 1.7 Ωcm and the thicknesses between 180 and 200 μm. Three fabrication processes have been used:

- **Process 1:** An ion-implantation process with homogeneous phosphorus doped emitter and an improved screen printing metallization step with fingers with a higher aspect ratio.
- **Process 2:** This process has been performed with a phosphorus diffusion step in a quartz tube furnace using liquid phosphorus oxychlorine ($POCl_3$) as the dopant source, and with wet chemical edge isolation. It benefits from a better optimization of the screen printing metallization step, giving fingers with a higher aspect ratio.
- **Process 3:** The standard process has been performed with an in line spray-on phosphorus diffusion step using phosphoric acid (H_3PO_4) as the dopant source.

The emitter sheet resistance is around 80 Ω/sq in all three cases.

Table 1 summarizes the features of the solar cells selected for this study.

Table 1. Review of the wafer's type, the fabrication process used and the efficiency achieved. The average values and standard deviations for the resistivity and the efficiency are also provided.

Substrate	Resistivity (Ωcm)	Fabrication Process	η (%)
EG-Cz-Si	1.5±0.1	2	17.9±0.3
EG-Cz-Si	1.3±0.1	2	18.8±0.4
UMG Quasi-mono – Si	1.1±0.1	3	16.0±0.3
UMG Quasi-mono – Si	0.9±0.1	3	16.6±0.3
UMG Quasi-mono – Si	0.8±0.1	1	17.9±0.4
UMG mc-Si	1.7±0.1	3	14.9±0.2
UMG mc-Si	1.7±0.1	3	15.2±0.3
EG-mc-Si	1.5±0.1	2	17.2±0.3
EG-mc-Si	1.2±0.1	2	17.9±0.3
UMG mc-Si	1.2±0.1	3	16.1±0.3
EG-mc-Si	1.0±0.1	2	16.7±0.2
UMG mc-Si	1.0±0.1	3	16.7±0.3
UMG mc-Si	1.0±0.1	2	17.6±0.3
EG-mc-Si	0.9±0.1	2	18.1±0.3
EG-mc-Si	0.8±0.1	2	17.8±0.3
UMG mc-Si	0.5±0.1	3	14.8±0.2

The substrate type, the resistivity of the wafers employed and the fabrication process are presented because it is going to be studied their effects on the temperature coefficients of the solar cells. In this sense, the firs column of the table shows the substrate type. Two neighbor solar cells have been selected in each case. Wafer resistivities have been obtained directly from the manufacturer and/or calculated with the PC1D simulation software [12]. The third column presents the fabrication process, exposed above, used in each case. Finally, the last column of the table shows the average efficiency obtained under standard test conditions in each case.

A statistical analysis of the temperature coefficients of a selected group of solar cells has been carried out. The temperature coefficients in this work are defined relative to values of the relevant solar cell electrical parameters when measured under standard test conditions. The most important results are presented below.

4. Results and discussion

The temperature coefficients of the main electrical parameters have been obtained from the IV curves at different temperatures using a class A solar simulator. The irradiance has been set to 1000 W/m^2, and under AM1.5G spectrum. The measurement takes less than 1/3 of a second. Therefore, the heating of samples during the characterization is negligible. Fig. 1 summarizes the average temperature coefficients and standard deviations of the solar cells against the wafer resistivity.

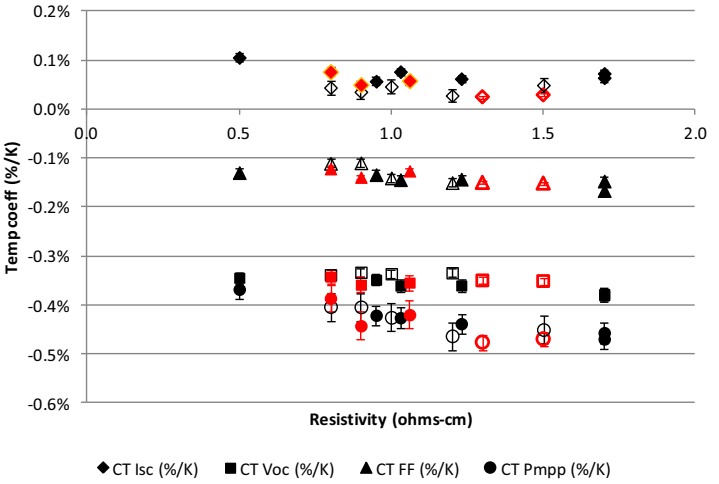

Fig.1: Temperature coefficient of the industrial solar cells selected against the wafer resistivity. Solar cells processed with UMG-Si wafers are represented with solid symbols. Open symbols are used to represent solar cells done with standard silicon wafers. Two colors have been used: black for solar cells done with multicrystalline silicon wafers, and red for monocrystalline silicon wafers, respectively.

MINITAB® Statistical Software has been used to analyze the temperature coefficients presented in Fig. 1. A factorial design has been selected to study the effects of the wafer type, its resistivity, the fabrication process and the electrical parameters of the solar cells on the temperature coefficients.

CT Voc: This is the parameter which has the highest influence on the variation of the solar cell's power with temperature. According to Fig. 1 and 2, and regardless of the wafer type used (mono or multicrystalline), the tendency found for UMG-Si solar cells is to a smooth and lineal decrease with the substrate resistivity. By taking in account measurement uncertainties, it has been obtained that this temperature coefficient is almost constant in EG-Si solar cells. According to Eq. (5), it can be justified considering that the relative variation of Jo with temperature is higher for UMG-Si substrates.

In our study, it has been obtained that solar cells manufactured with the processes 1 or 2 and with EG-Si wafers have a slightly lower temperature coefficient value. It is because solar cells processed with a better fabrication process have higher voltages (lower recombination) and therefore, lower variations of this parameter with the temperature [4,5]. In the same way, lower resistivities imply higher open circuit voltages [13] and according to Eq. (5) and (6), a lower variation of this parameter with temperature.

Comparing mono and multicrystalline solar cells with similar resistivities, and fabricated with process 2, this temperature coefficient is slightly lower for mc-Si solar cells in general, and for the EG-mc wafers in particular. We propose that this phenomenon is due to the implicitly higher dark current saturation in multicrystalline material due to much higher grain boundary interface recombination. The increase in bulk recombination is therefore relatively less important with increasing temperature. This point requires further work beyond the scope of this study.

With respect to the solar cell's open circuit voltage and regardless of the type of substrate used, it is clear that the variation of this parameter with temperature is lower as Voc increases. According to Eq. (4), higher Voc are presented in silicon solar cells processed with low resistivity wafers and/or with a lower effective recombination. Besides and taking in account Eq. (5) and (6), the variation of Voc with temperature is lower in both cases.

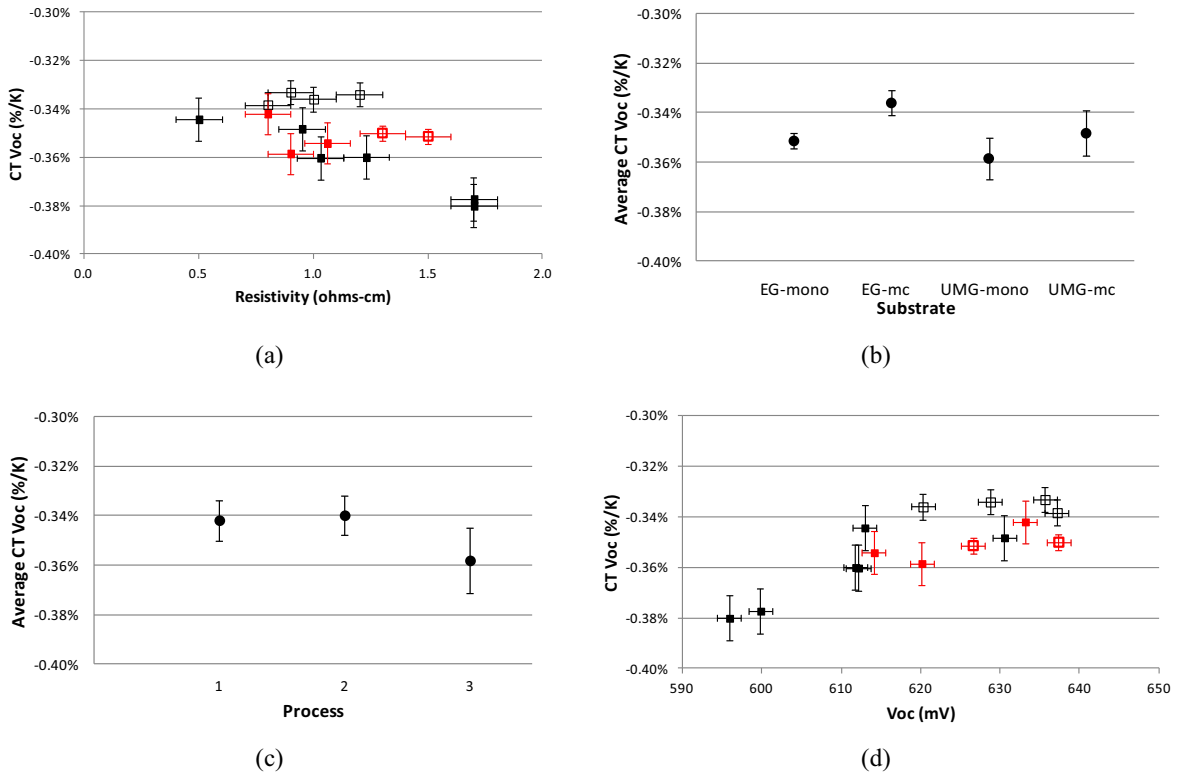

Fig. 2: Tendencies of CT Voc as a function of (a) the substrate resistivity, (b) type, (c) process and (d) Voc. Open symbols are used to represent solar cells done with standard silicon wafers. Two colors have been used: black for solar cells done with multicrystalline silicon wafers, and red for monocrystalline silicon wafers, respectively.

CT FF: The second parameter which has a higher relevance on the CT Pmpp is the temperature coefficient of the Fill Factor. Fig. 1 and 3 show that this value decreases again linearly with the resistivity of the substrate. For this coefficient, it has not been found notable differences between solar cells processed with EG or UMG, mono or multicrystalline silicon wafers. Acording to Eq. (7) and mainly due to the increase on the series resistance, the CT FF is worse in solar cells processed with a less optimized process and because of that, with lower FF.

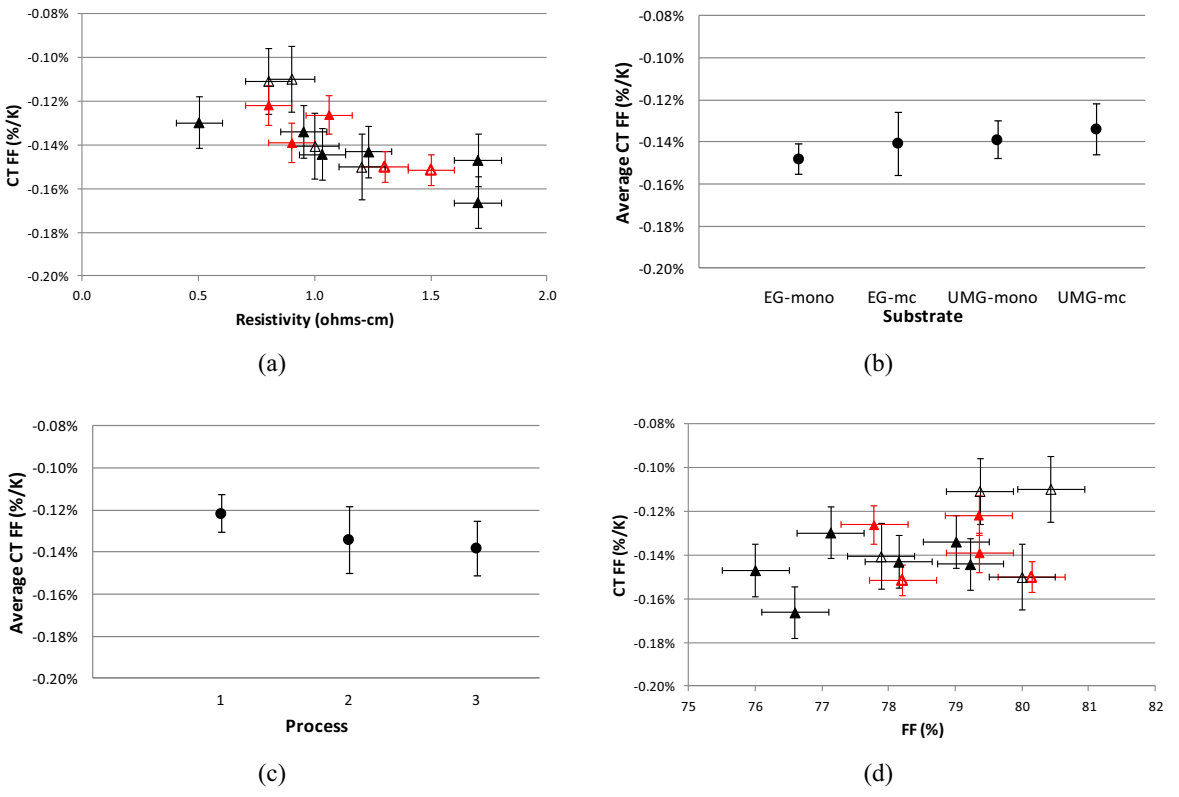

Fig. 3: Tendencies of CT FF as a function of (a) the substrate resistivity, (b) type, (c) process and (d) Fill Factor. Open symbols are used to represent solar cells done with standard silicon wafers. Two colors have been used: black for solar cells done with multicrystalline silicon wafers, and red for monocrystalline silicon wafers, respectively.

CT Jsc: Fig. 4 shows that the temperature coefficient of short circuit current depends mainly on the substrate type and its resistivity. The reduction of the band gap with temperature has a higher influence on low resistivity solar cells. Substrates with lower resistivities are often accompanied by a higher SRH recombination. Higher SRH recombination implies higher relative variations of the diffusion length with temperature [9]. Because of that, there is a large improvement on Jsc in solar cells with lower lifetimes (mc-Si vs mono-Si, and UMG-Si VS EG-Si). Furthermore, the reduction on the mobility of minority carriers with temperature is lower on UMG-Si wafers [2]. Because of that, UMG-Si solar cells have a better CT Jsc.

Fig. 4 (a) shows that high resistivity UMG-Si solar cells don't follow the expected trend. Their low efficiencies and Voc implies a high SRH recombination, which compensates the effect of the resistivity in CT Jsc.

Fig. 4 (d) shows that the variation of the short circuit current with temperature tends to decrease in solar cells with higher Jsc. Higher Jsc are presented in high resistivity solar cells and/or with higher effective lifetimes. Because of that, the effects of the band gap and/or the effective lifetime variations with temperature in Jsc are lower. There is a case with higher Jsc and CT Jsc which doesn't follow the trend presented by other solar cells. That one refers to the cells processed with low resistivity UMG-Si wafers and an ion-implanted phosphorus emitter. This result highlights the importance of the resistivity in CT Jsc.

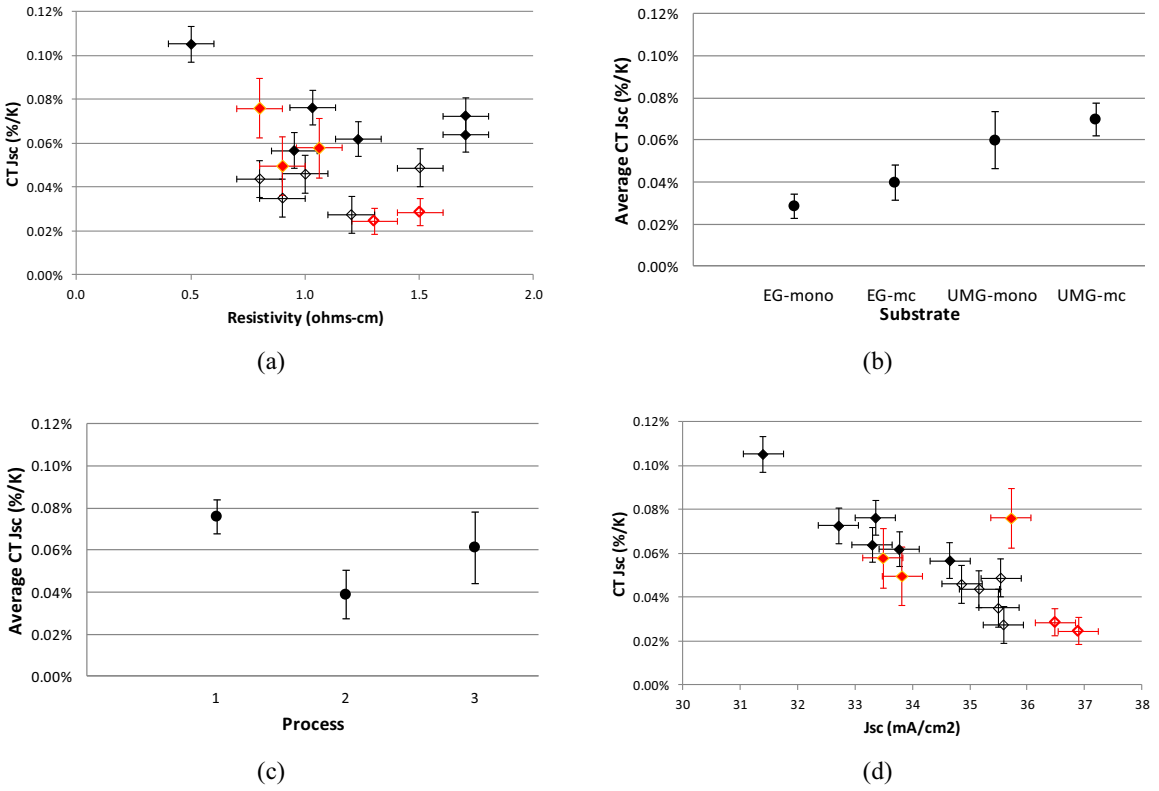

Fig. 4: Tendencies of CT Jsc as a function of (a) the substrate resistivity, (b) type, (c) process and (d) short circuit current density. Open symbols are used to represent solar cells done with standard silicon wafers. Two colors have been used: black for solar cells done with multicrystalline silicon wafers, and red for monocrystalline silicon wafers, respectively.

CT Pmpp: The tendency of the temperature coefficient of the maximum power depends on CT Jsc, CT Voc and CT FF. As shown in Fig. 5, and in accordance with the previous results exposed, the resistivity is the most important factor in CT Pmpp independently of the substrate used. Lower resistivities imply lower power variations with temperature. The reasons for this are complex. The band gap, first, is relatively unaffected by the doping levels involved here. The transport, however, is sensitive to doping density and leads to increased impurity-scattering dominated reduction in mobility, and increase in recombination. These effects both translate as a reduced temperature sensitivity due to transport increasingly dominated by impurities. This effect is, however likely to be slight although quantitative evaluations are beyond the scope of this paper. The built in potential, on the other hand, is slightly increased by higher doping levels in low resistivity devices, leading to lower dark current saturation currents and higher Vocs. Although an optimum doping level is a complex optimization of decreased transport and lower Jsc versus increased built-in junction potential and lower dark current, the consequence in this case is a reduced temperature dependence in the more highly doped samples.

Mainly due to the tendency found on the CT Jsc, the variation of the power with temperature is slightly lower for solar cells processed with UMG-Si substrates. Besides, the variation of the power with temperature for low efficiency solar cells is lower due to their higher SRH recombination losses.

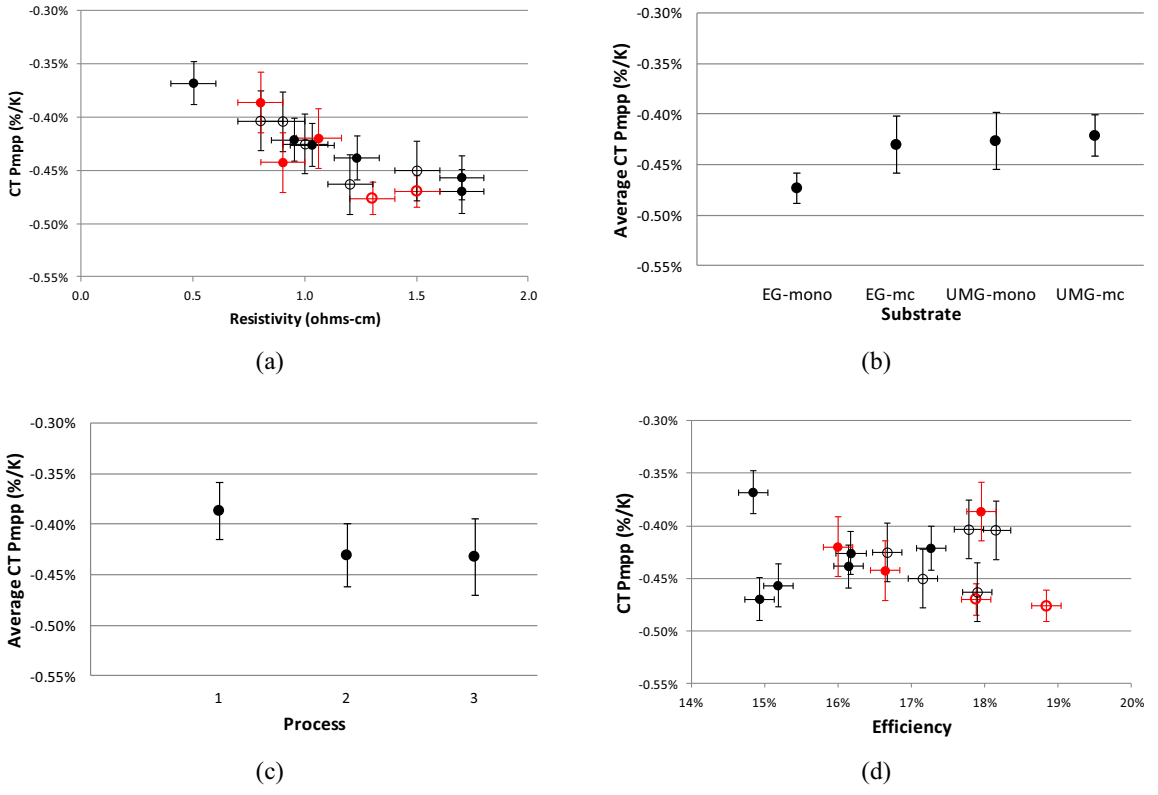

Fig. 5: Tendencies of CT Pmpp as a function of (a) the substrate resistivity, (b) type, (c) process and (d) efficiency. Open symbols are used to represent solar cells done with standard silicon wafers. Two colors have been used: black for solar cells done with multicrystalline silicon wafers, and red for monocrystalline silicon wafers, respectively.

A summary of the tendencies found on the temperature coefficients is shown in Fig. 6, which is a Pareto chart of the significant effects on CT Pmpp. The resistivity is the parameter with the highest influence. Regardless the type of wafer employed, lower resistivities give a better behavior against increasing temperature. The substrate type is the second effect to be taken in account. It has been found that solar cells processed with UMG-Si wafer in general, and with a multicrystalline wafer in particular, have a lower power variation with temperature.

The solar cell fabrication process has an influence on the temperature coefficients. Considering wafers from the same ingot and with similar resistivities, a high efficiency process gives solar cells with a higher effective lifetime. Therefore, according to Eq. 5, 6 and 7, the variation of Voc and FF with temperature is lower if a better fabrication process is used. On the other hand, those high efficiency solar cells have a small current increase with temperature. Conversely, the lower efficiency solar cells have a slightly worse CT Voc and CT FF. However, low efficiency solar cells in general and UMG-Si solar cells in particular have a high CT Jsc. It is mainly due to their lower mobility variation with temperature [2] and/or their higher SRH recombinacion, which gives a higher variation of the lifetime with temperature [9]. The improvement on CT Jsc compensates or even reduces the effect of the other temperature coefficients, producing a lower variation of the power with temperature.

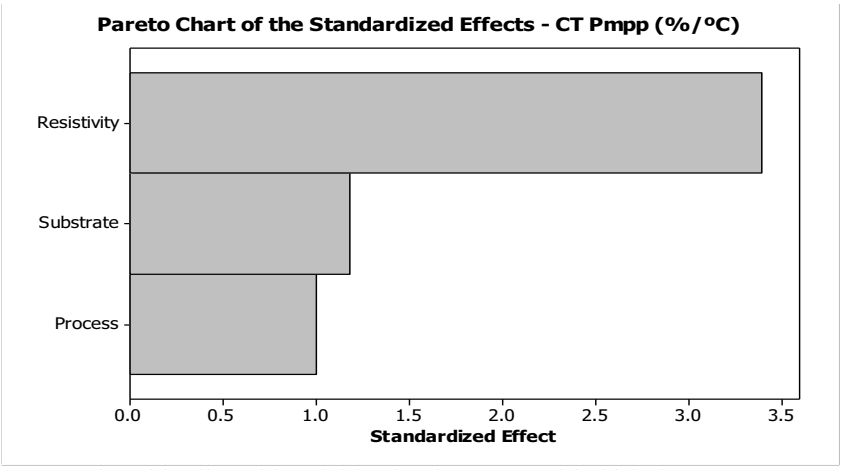

Fig. 6: Pareto chart of the effects of the resistivity, the substrate type and the fabrication process on CT Pmpp.

4.1. Temperature coefficients against the efficiency of industrial silicon solar cells

Another interesting tendency is found representing the temperature coefficients against the solar cell efficiencies. This is shown in Fig. 7.

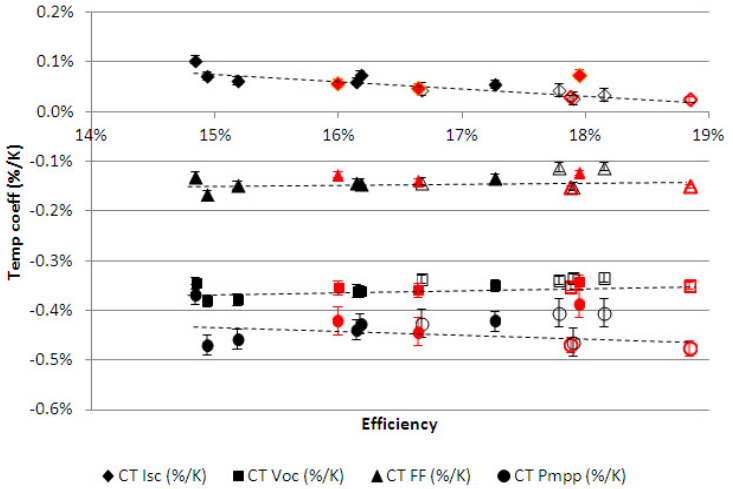

Fig. 7: Temperature coefficients against the efficiency of solar cells. Solar cells processed with UMG-Si wafers are represented with solid symbols. Open symbols are used to represent solar cells done with standard silicon wafers. Two colors have been used: black and red, for solar cells done with multicrystalline and monocrystalline silicon wafers, respectively. The lines are guides to the eyes.

There is a clear improvement on the CT Jsc for solar cells with lower efficiencies. As we have seen, it can be explained by the dependence of the SRH recombination [9] and the band gap variation [7] with temperature, joint to the lower effect of the temperature on the mobility of minority carriers in the case of UMG-Si solar cells [2,8].

The CT FF is not clearly correlated with the solar cell efficiency. Its value is almost constant, with slight variations depending on the resistivity of the substrate and the fabrication process used.

The tendency of the CT Voc is to improve slightly with efficiency. Higher efficiencies imply lower recombination and because of that, a lower impact in saturation current density variation with temperature.

Due to the use of different substrates, resistivities and fabrication processes, there is no direct relation between

the CT Pmpp and the efficiency of the solar cell.

Despite the slight improvement in CT Voc with the efficiency, the variation of the CT Jsc is higher. Consequently, following the dominant factor which is the tendency observed on the CT Jsc, we find that the variation of the power with temperature is lower for solar cells with lower efficiencies.

5. Conclusions

This work has studied the temperature coefficients of a number of silicon solar cells processed in a range of fabrication lines with EG and UMG, mono and multicrystalline silicon substrates.

For solar cells fabricated with wafers of comparable resistivities, the quality of the substrate and the fabrication process used have a significant impact on the temperature coefficient. An optimized fabrication processes is important in increasing the efficiency and reducing both the CT Voc and the CT FF. On the other hand, solar cells with lower SRH recombination show a lower improvement in photocurrent due to a relatively lower variation of the lifetime with increasing temperature. This effect partly compensates the improvement in CT Voc and CT FF.

Solar cells with a higher SRH recombinacion give a higher variation of the lifetime with temperature. Furthermore, the relative reduction of the mobility of minority carriers with temperature is lower for UMG-Si wafers. As a result, UMG-Si solar cells have a better CT Jsc, thus diminishing the effect of the temperature on power output. Therefore, the positive effect of the CT Jsc is responsible of improved performance of the UMG-Si solar cells as a function of temperature.

Concerning the variation of the temperature coefficients with solar cell efficiency, solar cells with lower efficiencies generally have a relatively worse CT Voc. This is however compensated by the observed variation of CT Jsc, which leads to an overall improvement in CT Pmpp.

These analyses conclude that solar cells with lower resistivities, processed with a high efficiency fabrication process and with UMG-Si substrates show the lowest variation of output power with temperature.

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