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***Abstract*—Low-cost devices with ultra-low power radio capabilities are a major challenge in smart devices, while a permanently-on receiver is required for smart communication. This paper proposes a wake-up radio with a neuromorphic pre-processing system both biased in weak inversion region. The system is able to receive a 2.4 GHz signal, demodulate it, and recognize bit patterns based on the spiking frequency of a neuron. Significant performance is obtained with 1.2 nW of total power consumption, which is at least three orders of magnitude less than the conventional RF envelope detectors. Further, spiking frequency responsiveness over input power suggests that the proposed system can distinguish different signals at 2.4 GHz. The proposed system achieves an energy efficiency of 1.2 pJ/bit with a minimum detectable signal of -27 dBm.**

***Index Terms*—envelope detector, neuromorphic sensor, IoT devices, ultra-low power.**

I. Introduction

The founding pillar of Internet of Things (IoT) concept is the availability of low-cost devices with ultra-low-power wireless communications capabilities [1]. A promising approach to dramatically reduce the power consumption is to use a permanently-on ultra-low-power receiver, a.k.a wake-up receiver. Whenever it detects a communication request, it wakes up the main radio of high performance from deep sleep to receive data. On-Off Keying (OOK) modulation is usually adopted with simple RF envelope detection to achieve low-power consumption. However, the minimum detectable signal by the receiver is limited by the quadratic nonlinearity of such detectors [2].

Furthermore, the approaching end of Moore's law and the increasing power demands limit traditional computing, such as Von Neuman's systems [3]. While Von Neuman architectures suffer from energetic and speed bottlenecks, neuromorphic systems come to achieve real-time performance and better power efficiency. In contrast to digital neuromorphic systems, analog solutions save significant power, thanks to their capability to faithfully mimic biological neural systems [4].

To explore the sensory processing in the brain, neuromorphic engineers have focused on mimicking the retina and cochlea [5]. However, a smart vision or audition in IoT requires an RF sensor system since IoT devices communicate through electromagnetic waves. With the increasing number of sensors and sensory systems in IoT, signal processing is becoming a problem due to the data complexity and the large number of devices. Thus, RF neuromorphic may drive a new generation of bio-inspired signal processing.

This paper aims to implement a novel RF architecture using neuromorphic sensing for IoT applications. The proposed method paves an innovative way for brain-inspired applications and hardware AI to explore new paradigms for neuromorphic sensors. Figure 1 illustrates the proposed system, which is designed in the BiCMOS SiGe 55 nm technology from ST Microelectronics. It consists of a wake-up radio system with a neuromorphic pre-processing system (comprising a synapse and a neuron). The system detects the RF input signal (V_{RF}), demodulates it (V_{ED}), and converts it into an excitation current (I_{ex}) connected to an artificial fast-spiking neuron (FS eNeuron). The overall system can detect and identify bit patterns of a 2.4 GHz OOK-modulated signal. Moreover, the proposal can also observe the electromagnetic environment and seize important informations. In this case, it is able to recognize the RF input power based on the spiking frequency (f_{spike}) of eNeuron.

This paper is organized as follows. General background is presented in Sec.II. Proposed system and each stage of it, with mathematics modeling, are described in Sec.III. Results of post-layout simulations are explored in Sec.IV to demonstrate the spike-based signal processing. Finally, conclusions are drawn in Sec.V.

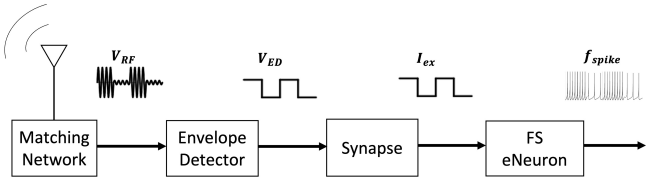


Fig. 1. Proposed RF neuromorphic sensor system composed of four stages: a matching network, an envelope detector, a synapse, and a fast-spiking eNeuron. Stages are detailed in Sec. III.

II. Background

A. Wake-up Receiver

IoT offers many opportunities in smart physical objects combining artificial intelligence and signal processing in low-cost context-aware devices. For many applications, IoT devices may require low power consumption. To meet this requirement, a hardware solution composed of two receivers is often used [1]. One is the main receiver with high performance and it is kept in a deep sleep until it is needed. The other is the

wake-up receiver (WuR) with ultra-low power consumption. The WuR is always on and asynchronous.

Most wake-up receivers implemented for sensor networks use a 2.4 GHz carrier (F_{RF}) and OOK modulation. Energy efficiency is defined as $E_{eff} = P_{rms}/DR$, where P_{rms} is the receiver's power consumption and DR is the data rate expressed in kilo-bit-per-second (kbps). Cheng *et al.* have proposed a wake-up receiver based on direct active RF detection [2]. At the operating frequency of 2.4 GHz with DR = 200 kbps, their RF detector achieves -50 dBm minimum detectable signal (P_{mds}) while consuming 2.4 μW. Besides, their receiver has an energy efficiency of 22.5 pJ/bit.

Recently, Kinget *et al.* have designed a wake-up receiver with gate-biased self-mixers [6]. It consumes only 420 pW with an interesting P_{mds} = -79.1 dBm. It achieves an E_{eff} = 4.2 pJ/bit. However, it operates at 434 MHz with DR = 0.1 kbps, which is a very low carrier and data rate for IoT applications. At 0.9 GHz and for a DR = 1 kbps, Karami *et al.* have proposed a wake-up receiver lately with a P_{mds} = -26 dBm and a low P_{rms} = 5.7 nW [7]. Based on that, 5.7 pJ/bit of energy efficiency is obtained.

Since the envelope detector is the part of the wake-up radio operating in RF, it is usually the main contributor to power consumption. A simple demodulator can be considered for that purpose, especially when the RF input is an OOK signal [8]. This paper proposes a simple envelope detector, as shown in Fig. 2.

B. Neuromorphic Analog System

Neuromorphic computing appeared in the 90s as a complementary architecture to Von Neuman systems [3]. It is spread in analog and digital domains. Neuromorphic analog systems take inspiration from biological neural systems and their reliance on physical properties for computation. The neuromorphic hardware approach consists of large-scale integration of silicon artificial synapses and neurons (eNeurons) [3]. In widespread literature, neuromorphic analog systems use circuitry that operates in the subthreshold mode for low power properties [4], [9], [10].

One of the synapse implementations focuses on unsupervised learning for synaptic weight updates through the spike-timing-dependent plasticity rules [3]. To build plastic synapses, emerging technologies such as memristors are used [11]. However, issues such as process variation and reliability are presented for unconventional technologies. Danneville *et al.* [9] have designed synapses using inverters to produce a long synaptic current pulse. Indiveri *et al.* have been one of the first to propose a silicon synaptic circuit in a spiking neural network. They have designed complex synapse blocks as an array implementation of current mirrors [12], where current mirror gains represent the synaptic weight. In this paper, a synapse model tends to be relatively simple, composed of two current mirrors, as shown in Fig. 2.

Various eNeuron models are implemented in hardware due to a trade-off between complexity and biological inspiration. Moris-Lecar model (ML) has presented a simple eNeuron while faithfully mimicking biological system [3]. Moving to a less biologically realistic category, the leaky integrate-and-fire model (LIF) has produced enough complexity in behavior to be useful in spiking neural systems. Spiking eNeuron is often compared in the state-of-the-art by its output spiking frequency f_{spike}, its power consumption $P_{rms,N}$ and its energy efficiency $E_{eff,N} = P_{rms,N}/f_{spike}$.

Sourikopolous *et al.* [4] have innovated biomimetic and simplified versions of the eNeuron model based on ML implementation. They have first demonstrated a 4 fJ/spike energy efficiency with a relatively constant period by reaching a maximum f_{spike} of 26 kHz. Danneville *et al.* have designed a low-power LIF eNeuron in a small surface area [10]. Its spiking frequency is 15.6 kHz and its energy efficiency is 2 fJ/spike. Recently, a fast-spiking (FS) eNeuron is designed in the previous work [13]. This FS eNeuron spikes with a higher firing rate to highlight a better energy efficiency trade-off. A maximum f_{spike} of 400 kHz and an $E_{eff,N}$ equal to 1.95 fJ/spike are obtained. Based upon this previous work, an FS eNeuron is redesigned from [13] to achieve a large band of spiking frequency in the system. It is shown in Fig. 2.

C. Neuromorphic Signal Processing

Neuromorphic signal processing opens a wide range of applications such as motion control, image recognition, and sensory detection [3]. A neuromorphic hardware system for visual pattern recognition is designed in [14]. It contains an artificial photoreceptor, which converts an image into voltage pulses, a memristor array for synaptic connections, and LIF neurons. Cassidy *et al.* have designed a wireless address event representation (AER) [15]. Cassidy's neuromorphic impulse radio introduced a distributed wireless cortex capability using a digital neuromorphic system (i.e., FPGA) and discrete RF components. In IoT applications, artificial sensing requires novel RF architectures for signal classification and real-time processing. However, RF architecture challenges in neuromorphic sensing are not addressed in the state-of-the-art.

III. Proposed RF neuromorphic sensor

The neuromorphic-enhanced WuR system level is illustrated in Fig. 1, while transistor-level description is available in Fig. 2. To address RF 2.4 GHz band, a 50 Ω matching network is required (not represented in Fig. 2). It consists of a capacitance and an inductance achieving a maximum power transfer. Figure 2 presents the envelope detector (M_{CG}) followed by a low-pass filter (C_{LP}, M_1). Excitation current I_{ex} is delivered by the synapse (Fig. 2) to the FS eNeuron (Fig. 2).

All transistors are operating in weak inversion region to take advantage of two things. First, an ultra-low-power consumption is obtained by a supply voltage around of ±100 mV (V_{DD} = 100 mV and V_{SS} = -100 mV). Secondly, in the ML eNeuron model, the generation and propagation of a spike seek an implementation of non-linear gating variables to control the ionic channel currents. Such behavior requires transistors operating in the subthreshold region [4].

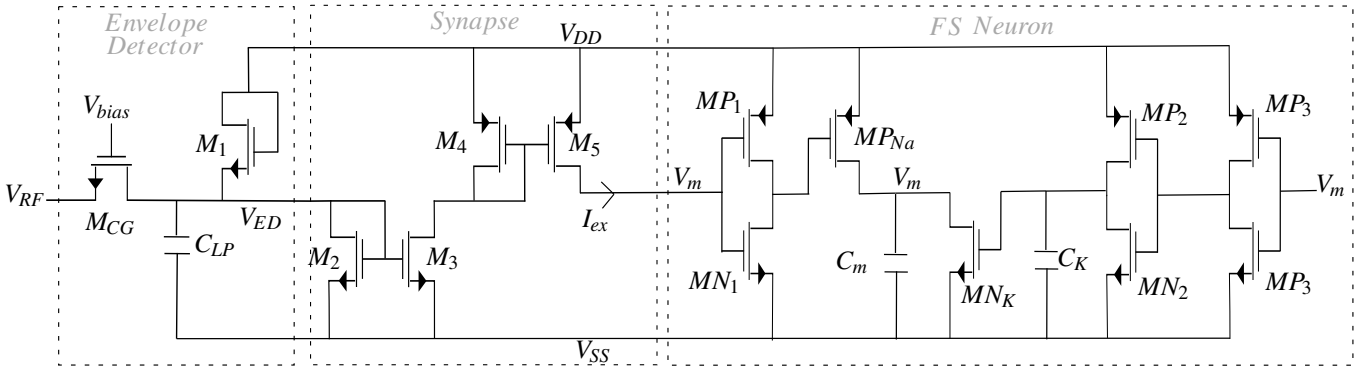


Fig. 2. Circuit level of the proposed system composed of an envelope detector, a synapse and an FS neuron (V_{DD} = 100 mV and V_{SS} = -100 mV)

A. Envelope Detector

RF envelope detector rectifies the incoming OOK signal V_{RF} and provides a baseband output V_{ED} equivalent to the envelope of the original signal. Three popular forms of RF envelope detector configurations are common drain, common gate, and common source [2]. In this paper, the envelope detector is a common gate transistor M_{CG} since it can achieve a maximal conversion gain [2]. The conversion gain of the envelope detector (CG_{ED}) is obtained from the ratio between the demodulated output signal V_{ED} and RF input signal V_{RF}. In common gate topology and for small-signal analysis, the conversion gain of the envelope detector is expressed as:

$$CG_{ED} = \frac{V_{ED}}{V_{RF}} = \frac{i_o r_o}{V_{RF}} = \frac{I_D r_o V_{RF}}{4\phi_T^2} \tag{1}$$

where r_o is the intrinsic output impedance, and i_o is the output demodulated current represented by the second-order term of Taylor expansion as:

$$i_o = \left(\frac{\partial^2 I_D}{\partial V_S^2}\right)\frac{V_S^2}{2} \tag{2}$$

and I_D is the drain current expressed in the weak inversion region as:

$$I_D = I_s \cdot e^{(V_G - V_{T0})/\eta\phi_T}\left(e^{-V_S/\phi_T} - e^{-V_D/\phi_T}\right) \tag{3}$$

where I_s is the specific current; V_{T0} is the bias-independent threshold voltage for $V_S = 0$; η is the subthreshold slope factor ($\eta \approx 1.34$ for the 55nm BiCMOS technology, calculated based on [16]); ϕ_T is the thermal voltage ($kT/q \approx 26\ mV$ at 27 °C); and V_G, V_S, V_D the voltages on the gate, the source and the drain of the transistor respectively.

An example of a common gate transistor is studied in Fig. 3 to observe the behavior of its conversion gain as a function of its operating region. Figure 3 shows two curves: the blue line presents the conversion gain calculated from 1 and the red line presents the conversion gain obtained from PSS simulation. CG_{ED} is maximized for a $g_m/I_D \approx 26\ 1/V$. It corresponds to a transistor operating in the weak inversion region, thus achieving low power consumption. Therefore, M_{CG} is designed

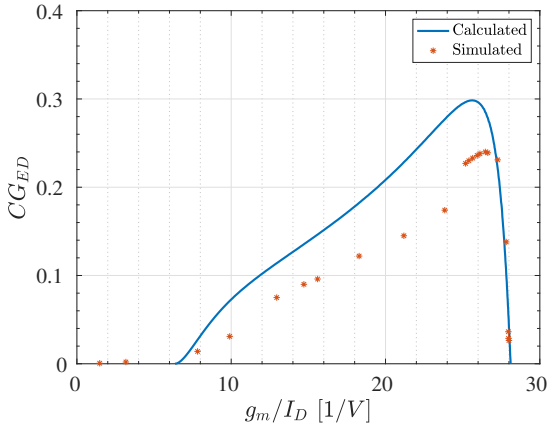


Fig. 3. Conversion Gain of the envelope detector as a function of gm/Id for a common gate transistor: the blue line is the calculated one and the red line is the simulated one.

on this region with a bias voltage V_{bias} = 300 mV, a length = 0.06 μm and a width = 0.13 μm.

Then, a low pass filter (LP) at the output of the envelope detector removes the high-frequency components. It is composed of a capacitance C_{LP} and a diode-connected transistor M_1. To reduce the silicon area of the system, the chosen capacitance is the smallest varicap-based presented on the BiCMOS 55nm technology. Dimensions are presented in Tab. I.

B. Synapse

In literature, the synapse is used in neural systems to translate pre-synaptic voltage pulses from a pre-neuron into post-synaptic currents to excite a post-neuron [9], [12]. In this paper, an excitatory synapse is implemented to generate the current I_{ex}. Thus, I_{ex} will excite the FS eNeuron differently according to the input power levels of RF signal. As shown in Fig. 2, the synapse consists of two current mirrors NMOS and PMOS. The purpose is to copy the output current of the filter through the active device and keep the output current I_{ex} constant regardless of the loading. Synapse sizing is shown in Tab. I.

C. FS eNeuron

Finally, an FS eNeuron based on ML model is connected to the system and is shown in Fig. 2. This biomimetic eNeuron has been redesigned from [13] with a high firing rate to increase the system's dynamic range. Optimized FS sizing is presented in Tab. I.

Briefly, when the FS eNeuron is excited by an I_{ex} current, the membrane capacitance C_m is charged through MP_{Na} and discharged through MN_K. This causes a large but brief change in membrane potential (V_m), which is referred to as action potentials (spikes) [4]. Indeed, transistors MP_{Na} and MN_K mimic the continuous exchange of Na-in and K-out ions through the cell membrane in brain activity. Two cascaded inverters MP_2/MN_2 and MP_3/MN_3 with MN_K implement a negative feedback loop and inverter MP_1/MN_1 with MP_{Na} implement a positive feedback loop.

TABLE I
CIRCUIT SIZING IN W X L FOR TRANSISTORS AND NUMBER OF CELL X UNITY FOR CAPACITANCES

M_1	135 nm x 60 nm	C_{LP}	1 x 8.5 fF
M_2	405 nm x 60 nm	M_3	135 nm x 60 nm
M_4	135 nm x 60 nm	M_5	135 nm x 60 nm
MP_1	135 nm x 60 nm	MN_1	200 nm x 60 nm
MP_2	1200 nm x 60 nm	MN_2	135 nm x 60 nm
MP_3	200 nm x 60 nm	MN_3	135 nm x 60 nm
MP_{Na}	800 nm x 60 nm	MN_K	1500 nm x 60 nm
C_m	1 x 9.83 fF	C_K	1 x 5.53 fF

IV. RESULTS AND DISCUSSION

A layout of the proposed RF neuromorphic sensor was designed in the BiCMOS SiGe 55 nm technology from ST Microelectronics, shown in Fig. 4. The image rendering tool described in [17] is used for a high-quality layout illustration. The proposed system occupies 9.8 x 22 μm^2 of silicon area and consumes 1.2 nW of power from a supply voltage $\pm$100 mV. In this work, transmission lines and RF connections are not included in the reported area. Post-layout simulation (PLS) results of the proposal are then presented. Thus, the system performance is validated using PSS combined with PAC, PNOISE, and PSP Virtuoso Spectre simulations.

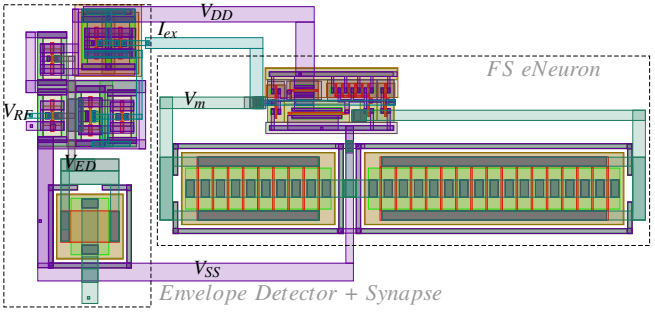


Fig. 4. The neuromorphic sensor layout (9.8 x 22 μm^2) presenting envelope detector, synapse, and FS eNeuron.

The analysis of the proposed system is divided into three parts. Firstly, to validate the functionality of the system, V_{RF}, V_{ED}, I_{ex}, and f_{spike} are shown from a transient noise PLS. Secondly, the dependency of V_{ED} and then I_{ex} on the input power levels P_{RF} are extracted from PLS. Therefore, the relation between input power levels and spiking frequencies of the eNeuron is deduced for both bits [0,1]. Finally, the system's specifications are defined: the gain, the power consumption, and the energy efficiency.

A. System Validation

A 2.4 GHz signal with different input powers (P_{RF}, in dBm) was connected to the system, and the output signal at each stage was observed. The RF input V_{RF} is an OOK modulated signal with a data rate (DR) of 1 kbps.

Figure 5 validates the system functionality where an average over eight transient noise simulations is considered. It illustrates the behavior of the system at different stages for a -10 dBm input signal. Simulations are carried out for three bits [0,1,0] in a window of 3 ms. That means a signal with zero voltage for bit=0 and a sinusoidal signal with an amplitude V_{RF} = $\pm$90 mV for bit=1. For the sake of better illustration, Fig. 5 presents the results in a limited range of time [0.5 ms : 1.5 ms] for two half bits [0,1].

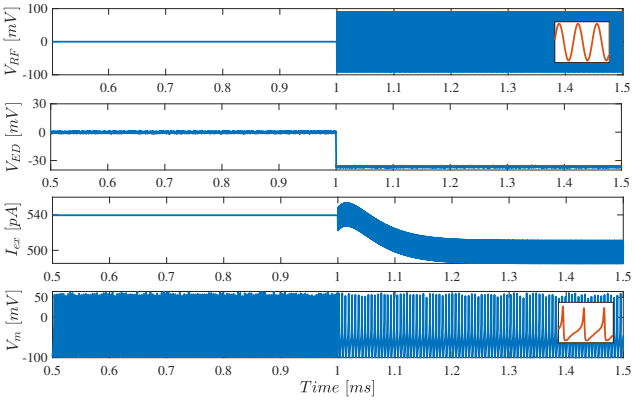


Fig. 5. Transient simulation that shows the response of the system for two half bits [0,1] at different stages: -10 dBm input signal V_{RF}, detected signal V_{ED}, excitation current I_{ex}, and membrane voltage V_m in respect to the time. A closer view is added for V_{RF} and V_m to clarify the sinusoidal and spiking behaviors respectively.

Two voltage levels of the demodulated signal V_{ED} are shown in Fig. 5: one for the bit zero data ($V_{ED,bit0}$ = 6 μV, near-zero and constant for any input power) and another for the bit one data ($V_{ED,bit1}$ = -36 mV, and varies with input power). Therefore, the excitation current is constant for the bit zero ($I_{ex,bit0}$ = 540 pA) and presents an average value for the bit one that differs with the input power. The spiking behavior of the membrane voltage V_m shown in Fig. 5 can be identified by f_{spike}. Besides, the spiking frequency of the eNeuron is obtained from the number of spikes in respect to the time (in this case, time of a bit is 1 ms). For -10 dBm input signal example, and for the bit one, $f_{spike,bit1}$ = 177 kHz. This value

varies with the input power as verified later in Sec. IV-D. However, for the bit zero and for any P_{RF}, the eNeuron spikes with a constant frequency equal to $f_{spike,bit0}$ = 254 kHz.

B. Envelope Detector

In order to assess the performance of the envelope detector presented in Sec. III-A , the minimum detectable signal P_{mds} (i.e., the sensitivity of the envelope detector) can be expressed as a function of the input power in dBm as:

$$P_{mds} = NF_{tot} + 10logB - 174 + SNR_{min} \quad (4)$$

where NF_{tot} is the overall noise figure of the circuit, B is the bandwidth of the envelope detector, and SNR_{min} is the minimum signal-to-noise ratio required by the OOK modulation for reliable detection. In this case, SNR_{min} = -12 dB and B = 10 MHz are considered.

As shown in Fig. 6, the sensitivity of the envelope detector is obtained from the intersection between the input power (P_{RF}, blue line) and the minimum detectable signal from 4 (P_{mds}, red line). The envelope detector presents a sensitivity of -27 dBm. Therefore, this value limits the gain of the overall system, as demonstrated later in Sec. IV-E.

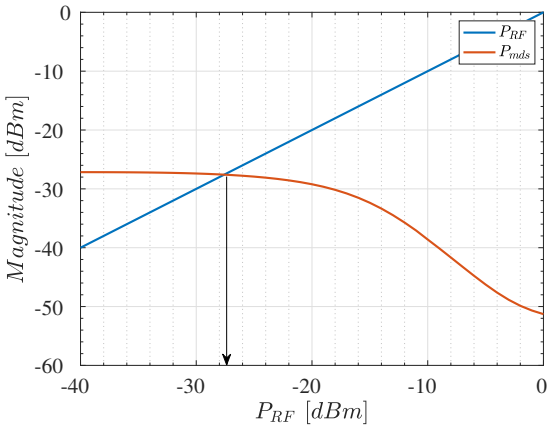


Fig. 6. Sensitivity of the envelope detector: the blue line is the RF input power P_{RF} and its cross with the red line is the minimum detectable signal P_{mds}.

A 31-point P_{RF} sweep is considered from -30 to 0 dBm for a 2.4 GHz input sinusoidal signal in Fig. 7. It illustrates the gain at each stage of the system: V_{ED}, I_{ex}, and f_{spike} versus P_{RF}. Indeed, Fig. 7(a) represents the variation of the demodulated voltage V_{ED} for a P_{RF} that varies from -30 dBm to 0 dBm for the bit one. One may notice that the P_{RF} sweep highlights the P_{mds} = -27 dBm.

C. Synapse

The exponential relation of V_{ED} with the input power P_{RF} shown in Fig. 7(a) for the bit one, in addition to the two current mirrors, lead to a decrement dependency of the excitation current I_{ex} on the power level as shown in Fig. 7(b). While P_{RF} increases from -30 dBm to 0 dBm, I_{ex} decreases from 420 pA to 12 pA.

D. FS eNeuron

When an FS eNeuron is connected to the system and excited by I_{ex}, its f_{spike} depends on the bit value and the input power. As the excitation current for bit zero is the maximum current delivered by the system to the eNeuron ($I_{ex,bit0}$ = 540 pA), its spiking frequency is considered the highest ($f_{spike,bit0}$ = 254 kHz). The reason behind that is to get the best energy efficiency of the eNeuron (in fJ/spike) for the bit zero as demonstrated in [13]. However, for the bit one, its spiking frequency varies proportionally with the excitation current in function of the input power. Figure 7(c) shows that f_{spike} decreases from 254 kHz to 25 kHz when P_{RF} increases from -30 dBm to 0 dBm. As expected, the eNeuron is always firing at $f_{spike,bit1}$ = 254 kHz for P_{RF} below -30 dBm, which is equal to $f_{spike,bit0}$.

E. System Performance

Assuming an uncertainty of 1 kHz spiking frequency between bit=0 (where $f_{spike,bit0}$= 254 kHz) and bit=1 in a window of 1 ms, the functionality of the system is validated until P_{RF} = -27 dBm where $f_{spike,bit1}$ = 253 kHz. As said before, the system's performance is limited by the P_{mds} of the envelope detector. Therefore, the system can distinguish signals at 2.4 GHz with input power levels between -27 dBm < P_{RF} < 0 dBm. Thus, the dynamic range is equal to 27 dB with a resolution of 1 kHz.

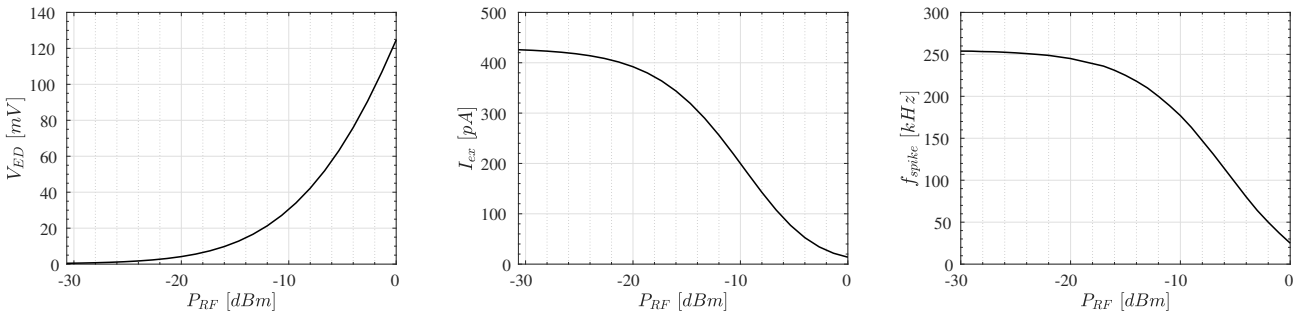
The overall system consumes 1.2 nW for the bit zero. The power consumption P_{rms} stays at an average of 1.2 nW for the bit one when P_{RF} is between -30 and -7 dBm. However, it increases until 11.2 nW for a 0 dBm signal power. The implemented FS eNeuron achieves an energy efficiency $E_{eff,N}$ between 2.5 and 5 fJ/spike depending on P_{RF}. Maximum f_{spike} achieved depends on the delivered I_{ex}. Such results are compared with the state-of-the-art of eNeuron in Tab. II.

State-of-the-art of envelope detector circuits target narrowband matching for low-noise circuitry, which leads to a low $P_{mds} \approx$ -50 dBm for high DR [2]. Besides, a low P_{mds} is demonstrated in spent of μW-range power consumption. Proposed neuromorphic sensor system achieves a P_{mds} = -27 dBm for only 1.2 nW of total power consumption. A better P_{mds} could be obtained if a narrowband off-chip matching network is chosen. The system presents a remarkable improvement in energy efficiency (E_{eff} = 1.2 fJ/bit) due to the neuromorphic enhancement. Table. II summarizes a literature comparison of envelope detectors.

It can also be noticed that the spiking detection was evaluated for one bit in an observation window of 1 ms and for a DR = 1 kbps. If a higher DR is chosen, one may reduce the observation window to 0.1 ms (DR = 10 kbps) or 0.01 ms (DR = 100 kbps) with no power consumption drawback. It is not the case in the state-of-the-art where a low P_{rms} and an interesting P_{mds} are achieved but only for a low DR [6].

V. Conclusion

RF neuromorphic sensor system remains a challenging issue for smart IoT devices. This paper proposed a neuromorphic



(a) (b) (c)

Fig. 7. Post-layout Simulations obtained for bit=1 for (a) the demodulated signal V_{ED} in mV, (b) the excitation current I_{ex} in pA, and (c) the spiking frequency f_{spike} in kHz in function of the input power P_{RF} varying from -30 dBm to 0 dBm.

TABLE II
ENVELOPE DETECTOR AND NEURON PERFORMANCE COMPARISON

Envelope Detector Performance					
Ref.	Techn. (nm)	F_{RF} (GHz)	P_{rms} (W)	P_{mds} (dBm)	E_{eff} (pJ/bit)
This Work	55	2.4	1.2 n	-27	1.2
[8]	130	2.4	120 n	-48.5	48
[2]	180	2.4	2.4 μ	-50	22.5
[6]	65	0.434	420 p	-79.2	4.2
[7]	130	0.9	5 n	-26	5
Literature eNeuron Performance					
Ref.	Model	Techn. (nm)	Area (μm^2)	f_{spike} (kHz)	$E_{eff,N}$ (fJ/spike)
This Work	ML*	55	103	457	2.5
[9]	LIF	65	31	15.6	2
[4]	ML†	65	200	1.2	78.3
[4]	ML‡	65	35	25	4
[13]	ML*	55	98.61	420	1.95

* fast-spiking † biomimetic ‡ simplified

enhanced wake-up radio as an innovative way for brain-inspired applications. It can identify bit patterns of a 2.4 GHz OOK-modulated signal and seize important information from electromagnetic environement. Thus, the system is able to distinguish different input powers based on the spiking frequency of the neuron. It occupies 9.8 x 22 μm^2 of silicon core area and consumes only 1.2 nW of power from a supply voltage $\pm$100 mV. Lastly, the system achieves a significant energy efficiency of 1.2 pJ/bit with a minimum detectable signal of -27 dBm.

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