Sub-nJ per Decison Schmitt Trigger Comparator for Neuromorphic Spike Detection in 55nm Technology

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Sorbonne Université, CNRS, Lab. de Génie Électrique et Électronique de Paris, 75252, Paris, France
Université Paris-Saclay,CentraleSupélec,CNRS,Lab. de Génie Électrique et Électronique de Paris,91192,Gif-sur-Yvette,France

***Abstract*—Neuromorphic circuits are known for their promising ultra-low power AI applications in IoT field. However, sub-100 mV supply voltages hamper digital-enable devices due to their non-discrete and highly non-linear response. In this paper, a low-power Smith trigger comparator is proposed to interface spiking analog eNeurons and digital circuits. To this end, a subthreshold bias and BiCMOS 55 nm node technology are chosen. The proposed comparator is post-layout validated, having a maximum decision frequency of 400 kHz and an energy efficiency of 747 aJ/spike. This performance is compatible with existing artificial neurons.**

***Index Terms*—Neuromorphic circuits, Schmitt trigger, spiking neural networks, ultra-low power**

I. Introduction

The hardware-based information processing, which is digital for the vast majority, is implemented in an architecture that has proven itself in terms of performance: computing power, memory capacity, and accessibility. Current architectures (e.g. Von Neumann, Harvard) were accompanied in their ascent by a manufacturing improvement in integrated circuits based on CMOS technology [1]. This technology has seen its performance growth, particularly in terms of miniaturization and heat dissipation, according to Moore's law. However, Moore's law undivided domination has hindered the emergence of purely neuromorphic solutions, whose first works started in the early 40's, and began to study technological solutions inspired by the brain's functioning. The end of Moore's Law observed since 2005 [2] brought back the interest by the neuromorphic approach, and open the way to the concept of bio-inspired engineering. Such solutions consist of new electronic solutions based on the observation of living things in order to analyze, in a short time and with extremely low energy consumption, complex situations.

Recently a mixed-signal approach in [3] combines the advantages of analog and digital solutions, being relevant for bio-inspired engineering. This scientific approach would induce a new class of ultra-sober and interconnected sensors, which is already finding concrete achievements in the field of the design of silicon cochlea [4]. Recent publications on artificial cochlea applications, as [5] [6], focus on intelligent acoustic sensing that combines high energy efficiency and signal processing capabilities such as spiked neural networks (SNN).

The SNN has been considered as the third generation of neural networks for its high biomimicry of the human brain [7]. The main difference between conventional artificial neural networks (ANN) and the SNN is that it processes spike trains instead of digital signals. One advantage of the SNN, thanks to its better mimicry of the biological behavior of the brain cortex, is that the development of an artificial intelligence (AI) system based on SNN has more potential to be inspired by the brain behavior. As the research on brain science is advancing rapidly, the process of inference and decision-making of the human brain can bring more and more inspiration to AI. Moreover, the SNN has lower energy consumption thanks to its event-driven property [8]. Not like neurons in ANN which are always kept active for data processing and memory access, a neuron in SNN shall be active only when it fires a spike. This event-driven property results in a giant reduction on computational consumption. The SNN is believed to have over 100 times higher efficiency on energy consumption than the ANN when implemented on a field-programmable gate array (FPGA) [9].

The SNN can be further energy-efficient on non-von-Neumann computing hardware as shown in [10]. In [11], the analog circuits of the two neuron cortex are designed according to Izhikevich model [12]. Operating with a higher spike frequency than that found in the literature [13], these artificial neurons respond to the relevant requirements in terms of silicon area (20×20 μm^2) and energy efficiency ($<$3 fJ/spike). In the following, a neuromorphic analog signal processor using a spike modulator has been proposed in [14]. From post-layout simulations, this device has proven to be able to encode the amplitude of an audio signal into a frequency of spikes and also to estimate its derivative for a silicon area of 24.5×15.5 μm^2 and energy efficiency of 8 fJ/sample. However, analog solutions have presented several reliability challenges in terms of process, temperature, and voltage variation, which are frequently overcome by digital solutions. These silicon neurons exhibit the useful behavior of converting analog information in their spiking frequency,

hence having useful signal processing properties for spike frequency modulation (SFM). However, this information is not directly useful for most applications, since the output wave form is often a non-linear combination of exponential functions. Thus, one needs to extract the information in the spiking frequency and generate a signal that can be directly used by the digital circuit. This paper proposes a spike detector that generates a pulse as an output, which is suitable to subsequent digital counter that estimates the number of spikes over a time span. Thus, the analog input can be fully converted in a frequency measurement without any analog-to-digital converter, whose dynamic range and refresh rate can be modified according to the designer's needs. The spike detector is a comparator based on a simplified non-inverting Schmitt Trigger topology to detect the spikes of a Morris-Lecar artificial neuron response.

Different topologies for Schmitt Trigger circuits have been proposed for low-power applications [15]–[18]. Some of them rely on positive feedback to generate better hysteresis loop qualities [19]. One recent proposition was made with adjustable hysteresis loop threshold voltage based on body-bias voltage controlling while offering a reduced number of six transistors [20]. This reduction is aligned with the power consumption and area constraints of neuromorphic circuitry, being a good candidate for further applications. Furthermore, the correct operation of a Schmitt-trigger topology in the weak inversion domain has been shown [21], allowing for more subthreshold applications.

In Section II, some propositions for neuron models as well as the respective state-of-the-art artificial neuron characteristic will be revised to appropriately define design specifications. In Section III, simplified Schmitt Trigger topology schematics and layout will be presented. In Section IV, the post-layout simulation results for nominal operation will be detailed. Finally, a conclusion is given in Section V.

II. Neuron Models

In the biological behavior of a neuron in brain cortex, the passing of Sodium (Na^+) and Potassium (K^+) or Calcium (Ca^+) ions generate current and membrane voltage, which fires spikes waveform of the membrane voltage. Different models have been proposed to describe this procedure, such as Moris and Lecar (ML) model [22], Izhikevich model [12], etc. In [23] and [14], the circuits of both FS and LTS neurons were designed based on ML and LIF models.

The various neurons mathematical models differ by their modeling complexity and their respective proximity to the real biological behavior of neurons. These models have different state-of-the-art circuit implementations that exhibit a varying electrical complexity. This change in electrical complexity plays a fundamental role in the performance, surface area and overall power consumption of the artificial neurons. As stated above, the chosen mathematical model for this work is the one proposed by Morris-Lecar, which is detailed below.

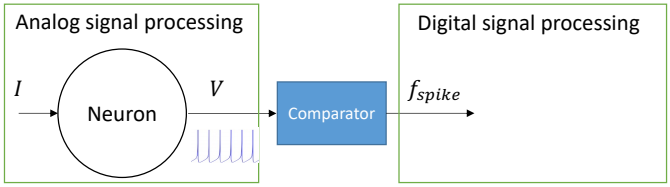

Fig. 1. A system scheme of a neuron with a comparator.

A. Mathematical Model

The Morris-Lecar model [22] is based on a system of three non-linear differential equations as (1) that models the time response of the membrane voltage of the neuron. The dynamic description is based on an external excitation current injected in the neuron and the opening of the Calcium and Sodium ion pumps that regulate the response. The output is often modeled by a voltage across the neuron's membrane.

$$\begin{cases} I = C\dot{V} + g_L(V_L) + g_{Ca}M(V - V_{Ca}) + g_kN(V - V_k) \\ \dot{M} = \lambda_M(V)[M_\infty(V - M)] \\ \dot{N} = \lambda_N(V)[N_\infty(V - N)] \end{cases} \tag{1}$$

In these equations, I corresponds to the applied external current, V to the membrane voltage and the others are modeling parameters relating to the dynamics of the ion channels.

B. Neuron system with comparator

In (1), the differential equation of membrane voltage V shows its gradient is negatively proportional to its own value, which means V increases slowly when its value is large. However, under the excitation by a current I which is large enough, the gradient of V is kept positive. The membrane voltage of a neuron keeps increasing till a threshold voltage and then abruptly resets to the rest voltage. This procedure generates a spike.With the existence of I, the neuron keeps on generating spike train with a frequency related to the value of I.

As illustrated in Fig 1, a comparator is connected behind the neuron to acquire digital information of the spike frequency f_{spike}. The system of a neuron circuit can be schematically illustrated as Fig 1. The output of the system in Fig 1, the spike frequency f_{spike}, increases non-linearly along with the value of I.

C. State of the Art Artificial Neurons

Most recent work carried on the field of silicon neurons have similar circuit topologies but with differences in the integration technology and transistor dimensioning. The major breakthrough for state-of-the-art performance is the use of MOS transistors in the weak inversion domain, which naturally reduces power consumption by limiting the supply voltage and current. Moreover, it offers exponential drain to source currents, which is convenient for the non-linear response of neurons. This allows to achieve an extremely low power consumption with only a few number of transistors and thus

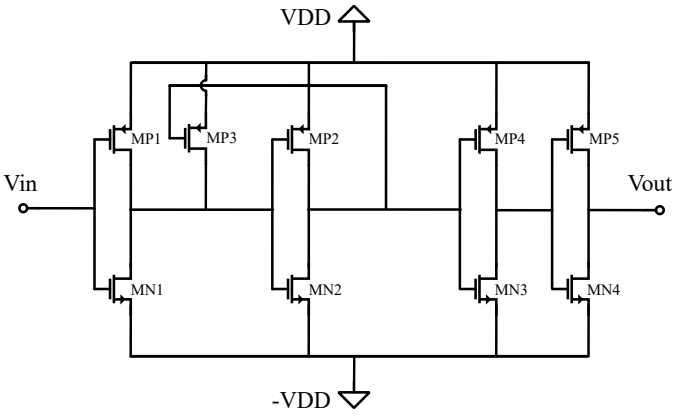

Fig. 2. Schematics of the full comparator.

with small area layouts, while still having an appropriate bio-inspired response. In [14] [23], electronic neurons exhibit an energy consumption in the order of few fJ/spike. It is thus desirable that other neuromorphic circuit blocks are aligned with this consumption, keeping the entire system in the ultra-low-power range. Besides, the threshold voltage that characterizes the event of a spike typically falls into the range 25mV-30mV, while the rest potential after recovery is a negative value of around -80mV. This is another important design constraint which shall be respected.

III. Simplified Schmitt Trigger for Neuromorphic Applications

A. Schematics

Fig. 2 illustrates the proposed spiking detector schematic. In this paper, we propose a comparator circuit which simplifies the previous non-inverting Schmitt Trigger topology of [14] by removing the negative feedback transistor, reducing the number of transistors to five. Moreover, the circuit was set to operate with a supply voltage V_{DD} of the order of 100 mV, moving the operation point to the weak inversion domain. This is the physical reason why the body-bias technique was not considered in this approach, as small variations could jeopardize the circuit's operation in this domain. Additionally, a buffer composed of two minimal inverters was added to the output of the Schmitt Trigger, allowing for output signals with better waveform characteristics.

One can see that the transistors MP1, MN1, MP2, and MN2 form two pairs of inverters, while the MP3 transistor remains as the positive feedback of the Schmitt trigger. The designer may then change the transition levels of the output by varying the W/L ratio between the transistors with different effects on each pair. In general, the first pair (MP1, MN1) changes the lower threshold of the comparator, while the second (MP2, MN2) changes the upper threshold. For each pair, increasing the ration in aspect of PMOS tends to augment the inverter threshold, while an increase in this parameter for the NMOS has the opposite effect. Due to the difference between the mobility of electrons and holes, the effect for n-channel transistors is usually heavier. The positive feedback transistor MP3 plays a major role in the circuit. Firstly, it provides the hysteresis cycle itself, which allows for a lower and an upper threshold. Secondly, it enables very fast changes in the output with respect to the input, which is a Schmitt-trigger fundamental characteristic. It is important to point out that all the relationships are non-linear and sensibly differ from layout results due to the exponential characteristic of the weak inversion operation. The final transistor dimensions are given in Table I.

TABLE I
Transistor Dimensions of the Full Comparator

Circuit part	Transistor Name	Width (μm)	Length (μm)
Schmitt-trigger	MN1	1.3	0.06
Schmitt-trigger	MN2	0.135	0.06
Schmitt-trigger	MP1	0.135	0.06
Schmitt-trigger	MP2	0.135	0.06
Schmitt-trigger	MP3	0.6	0.06
Buffer	MN3	0.135	0.06
Buffer	MN4	0.135	0.06
Buffer	MP4	0.135	0.06
Buffer	MP5	0.135	0.06

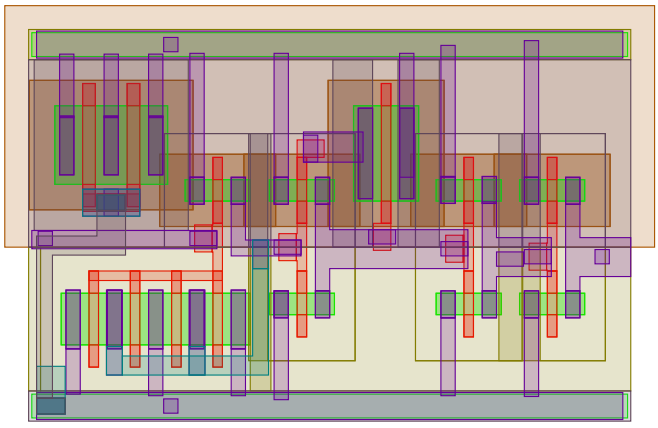

Fig. 3. Layout of the full comparator.

The lower threshold is obtained by sensibly increasing the aspect ratio of the NMOS of the first inverter (MN1). The global behavior of the circuit is adapted by varying the positive feedback transistor dimensions (MP3).

B. Layout

The layout of the proposed circuit is depicted below in Fig. 3 sizing 3.68 x 2.35 μm^2. The details can be seen in [24]. One important point to remark is the division of the largest transistor in several fingers to reduce overall area consumption. Moreover, an additional varicap connected PMOS transistor in the top left is included in the remaining area for direct current (DC) decoupling, which improves the general performance.

IV. Post-Layout Simulation Results

A. Hysteresis Cycle

One of the main features of the comparator is the hysteresis cycle. Having an appropriate value for turning on and off the output allows to correctly detect the event of a spike of the

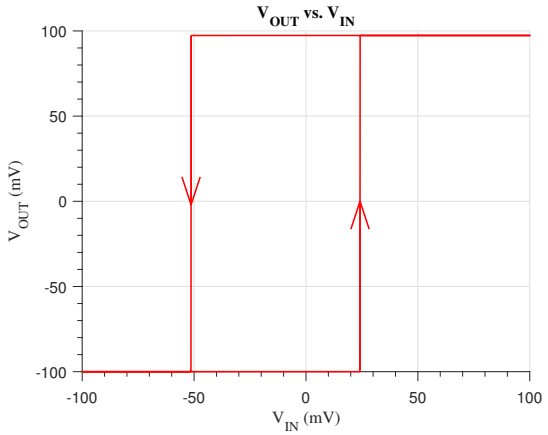

Fig. 4. Post-layout simulation V_{IN} vs V_{OUT} hysteresis cycle.

neuron. To verify the behavior of this cycle, a post-layout simulation was conducted using a DC analysis with an input sweep from -100mV to 100 mV with a 0.1 mV step and a grounded reference. For simplification purpose, no load is considered at this point. Fig. 4 illustrates the PLS result of the hysteresis cycle, where V_{IN} vs V_{OUT} represent the input and output voltage respectively.

As it can be seen in Fig. 4, the transition occurs with a very small variation of the input, with that being of the order of the sweep step (0.1 mV). The input for the high transition (V_{on}) was 24 mV and for the low transition (V_{off}) was -51 mV, both obtained for the midpoint between high and low output levels. Meanwhile, the output high (V_{high}) was 97.3 mV and the output low (V_{low}) was -100 mV, which is close to the 100 mV symmetrical supply voltages. While the positive threshold is very close to the typical range, the negative does not differ significantly, especially when considering that the voltage falls after a spike in a very sudden way. These values are thus coherent with the activation and rest potential of the Morris-Lecar neuron model as in (1). Though the output value is close to the supply voltages, a small drop still makes them discernible. Therefore, the hysteresis cycle allows the correct detection of spikes in terms of DC transition.

B. Propagation Delays and Output Settling Times

The DC analysis helps to establish the correct output/input behavior of the comparator in terms of threshold for spike detection. However, any insight into the time behavior of the circuit block is not accessible. In this case, the transient simulation is proven useful to extract most of the time domain characteristics, such as delays and dynamic power consumption. For this, the input was considered as a square wave with a high and low level of 25 mV and -81 mV respectively. This can be seen as a simplified model of the neuronal exponential response, which allowed more efficient simulations.

Firstly, the limit operation condition of the comparator regarding the duty cycle is verified for metastability issues. This is done by varying progressively the input duty cycle and checking the minimum values allowing to reach 90% of the stable output level. Two main classes of time-domain characteristics are analyzed: input/output propagation delays (LH and HL transitions) and output settling time (rise and fall). The results are summarized in Table II. Regarding the propagation delays, one can see that LH transitions present a lower delay than that of HL transitions. This is also the case for the output settling time, where the time for the output rise is much lower than the output fall. To completely avoid metastability issues, one can fix the circuit limit operation as the sum of the propagation delays and the output settling time. This yields a maximum operating frequency of the comparator in order of 400 kHz, which usually provides enough dynamic range for the representation of artificial neuron inputs in the spiking frequency [14].

TABLE II
DELAY AND SETTLING TIME CHARACTERISTICS

Type	Condition	Value
Propagation Delay	Low-High Transition	545 ns
Propagation Delay	High-Low Transition	939 ns
Output Settling Time	Rise	365 ns
Output Settling Time	Fall	830 ns

C. Eye Diagram

Considering this maximum frequency of operation of the comparator, the next transient simulations are carried on by fixing the period to 1.2 μs. Additionally, a noise analysis is introduced. The band for noise integration is established at least from the 5th harmonic, allowing a good trade-off between precision and simulation cost. Having an input frequency of about 5 MHz, this band is defined to have cutoffs at 5 MHz.

The main feature analyzed with the transient noise simulation is the eye diagram. Having the limit operating condition of the comparator in terms of frequency, this diagram provides a graphic representation of the output discernible levels and their transition. Therefore, it allows a fast verification of the circuit's operation. The result can be seen in Fig. 5. The analysis of Fig. 5 yields an eye width of 0.4 μs and an eye height of 200 mV. Despite operating in a fixed limit condition, the output remains stable for a reasonable amount of time. The eye height is close to the supply voltage, which indicates that the output levels are very discernible. This result is useful for the circuit designer to establish the design constraints for the digital circuit block at the output.

D. Power and Energy Consumption

Power consumption is one of the most important factors in the design of neuromorphic systems. The power consumption of the entire comparator (Schmitt trigger and buffer) is evaluated using the DC and the noise transient simulation. These simulations can emulate the power consumption of the circuit block in condition of high-spiking frequency. These results are presented in the Table III, both for static and dynamic root mean square (RMS) power. The static and dynamic powers are in order of pico-Watts, which renders the circuit operating in the ultra-low-power region. The static power consumption

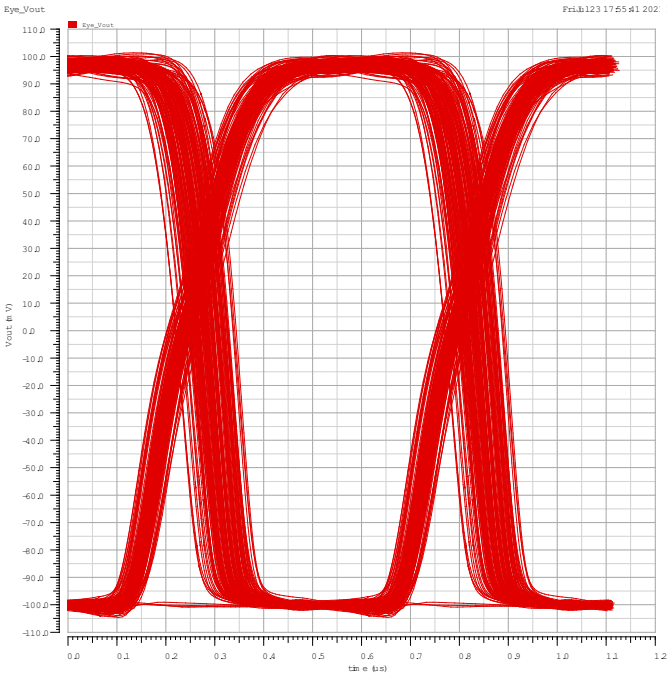

Fig. 5. Eye Diagram of Vout.

TABLE III
DYNAMIC AND STATIC POWER CONSUMPTION OF THE COMPARATOR

Type of Power	Condition	Value
Static	Low Output	58 pW
Static	High Output	31 pW
Dynamic	Low-High Transition	492 pW
Dynamic	High-Low Transition	199 pW
Dynamic	Complete Cycle	400 pW

is much lower than the dynamic consumption, as it is expected for CMOS inverters, thanks to the bigger amount of current that flows in the switching between the states. Moreover, the power consumption of the proposed comparator is smaller than that of most existing artificial neurons in the literature, which validates its performance in aspect of the circuit complexity and confirms its role as an intermediary circuit block.

Given the neuromorphic application of the circuit, one important and frequently used figure of merit (FoM) is the energy efficiency. This FoM is usually measured in fJ/spike, giving an insight about the energy per unit of information. Since one spike in the input should correspond to one low to high and high to low cycle, this FoM is also appropriate for this application. According to Table IV, the comparator has an aggregate energy efficiency of 0.7 fJ/spike. This well qualifies

TABLE IV
ENERGY CONSUMPTION OF THE COMPARATOR

Condition	Value
Low-High Transition	0.47 fJ/spike
High-Low Transition	0.28 fJ/spike
Complete Cycle	0.75 fJ/spike

it for ultra-low-power consumption, one of the requisites for this kind of neuromorphic system. Moreover, most of the artificial neurons in the literature have an energy efficiency around several fJ/spike, as previously presented. The comparator has a consumption that is of the same order of magnitude, hence being adequate to its role as a terminal block of the circuit. For an application of electronic neuron such as in [25] where a non-linear neuron is used for mathematical modeling of power amplifiers behavior, the output information of a neuron can be represented by hundreds of spikes, which consumes lower than 1 nJ per decision.

V. CONCLUSION

Neuromorphic circuits are gradually sparking more interest due to their potential of powerful information processing while having ultra-low power consumption and small surface area. Their effective use and direct application rely, however, on a circuit block that can be the interface between analog waveform of neuronal response and the discrete nature of digital signal processing circuits. With a BiCMOS 55 nm technology and subthreshold operation, this paper presented an energy efficient comparator that is suitable for Morris-Lecar based artificial neurons, having an energy efficiency of about 747 aJ/spike and a limiting frequency in the order of hundreds of kHz. The consumption of the proposed comparator during the information processing of a neuron is less than 1 nJ per decision.

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